MODELLING AND OPTIMIZATION OF SUBTHRESHOLD LEAKAGE CURRENT IN LOW-POWER, SILICON-BASED, COMPLEMENTARY METAL OXIDE SEMICONDUCTOR (CMOS) DEVICES

BY

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DECLARATION

Declaration by the Student

This thesis is my original work and has not been presented for a degree in any other University. No part of this thesis may be reproduced without the prior written permission of the author and/ or University of Eldoret, Kenya.

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DEDICATION

I would like to thank my family to which I dedicate this work.

ABSTRACT

The trend of process scaling for CMOS technology has made subthreshold leakage reduction a growing concern for submicron circuit designers. Power consumption has become a principle design consideration as device sizes decrease and many more devices fit on a single chip. Since switching power is proportional to the square of the supply voltage, V^{2}_{dd}, new processes are tailored for lower supply voltages. The decrease in V_{dd} slows down devices, which requires that the threshold voltage, V_{th}, must be lowered to maintain performance. This reduction of V_{th} produces the exponential increase of subthreshold leakage currents. This research demonstrates a process used to model and optimize subthreshold leakage current for a CMOS device during its standby mode (OFF-state). The process involves the use of MATHCAD to examine the OFF-state subthreshold leakage current, I_{sub} (OFF), based on variations in the threshold voltage, V_{th}, the effective transistor channel length, L, and the effective transistor channel width, W. The theoretical work entails simplifying the empirical relationship between the surface inversion potential, φ_s, the gate-source voltage, V_{gs}, and the Subthreshold swing coefficient, n. This results in an expression relating the OFF-state subthreshold leakage current, I_{sub} (OFF), the threshold voltage, V_{th}, the effective transistor channel length, L, and the effective transistor channel width, W. Analyzing the resulting equation using MATHCAD confirms that the OFF-state subthreshold leakage current, I_{sub} (OFF) increases exponentially with a decrease in the threshold voltage, V_{th}, and linearly with a decrease in the effective transistor channel length, L. The results also show that the OFF-state subthreshold leakage current, I_{sub} (OFF), increases linearly with the effective transistor channel width, W. The optimization process resulted in the values of V_{th} = 140 mV, L = 28 nm and W= 7 nm which give the desired outcome of greatly reduced OFF-state subthreshold leakage current, I_{sub} (OFF) = 0.125 nA, for a single transistor. Field Programmable Gate Arrays (FPGAs) are one type of chip that could benefit from such subthreshold leakage reduction techniques.

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ABBREVIATIONS, ACRONYMS AND SYMBOLS

C_L:	Load Capacitance
V_{dd}:	Supply Voltage
A:	Ampere
b:	Bulk or Substrate
BGMOS:	Boosted Gate CMOS
BSIM MOS:	Berkeley Short-Channel IGFET Model for MOS transistors
BTBT:	Band-To-Band Tunneling
C_b:	Bulk (Substrate) capacitance
C_{dep}:	Capacitance of the depletion layer
C_g:	Gate capacitance
CMOS:	Complementary Metal Oxide Semiconductor
C_{ox}:	Gate oxide capacitance
CPU:	Central Processing Unit
d:	Drain
DIBL:	Drain Induced Barrier Lowering
E:	Electric field
ECB:	Electron Conduction-Band
eV:	electronvolt
EVB:	Electron Valence-Band
FET:	Field Effect Transistor
FPGAs:	Field Programmable Gate Arrays
g:	Gate

GIDL: Gate Induced Drain Leakage

GND: Ground (Earth)

h: Planck's constant

ħ: $\frac{1}{2\pi}$ times the Planck's constant.

HVB: Hole-Valence-Band

IC: Integrated Circuit

$I_{d(weak)}$: Drain current in the weak or subthreshold regime

IEEE: Institute of Electrical and Electronics Engineering

IGFET: Insulated Gate Field Effect Transistor

I_{sub} or I_{sub}(OFF): Subthreshold Leakage Current

J: Current density

J_{ECB}: Electron-Conduction band Tunneling current density

J_{EVB}: Electron-Valence band Tunneling current density

J_{HVB}: Hole-Valence band Tunneling current density

k: Boltzmann's constant; $1.38 \times 10^{-23} \mathrm{J/mol.K}$

K: Body effect model parameter

L: Transistor effective Channel length

MATHCAD: Modelling software

MOS: Short for MOSFET

MOSFET: Metal Oxide Semiconductor Field Effect Transistor

MTCMOS: Multi Threshold CMOS

Ŋ: Drain Induced Barrier Lowering (DIBL) Coefficient

NAND: Not AND logic gate

N_{CH}:	n-channel
NMOS:	n-channel MOSFET
PMOS:	p-channel MOSFET
q:	Electronic Charge
S:	Subthreshold swing
s:	Source
SCCMOS:	Super Cut-off CMOS
SCE:	Short Channel Effect
SiO_2:	Silicon dioxide
SOI:	Silicon-on-Insulator
t_{ox}:	Gate oxide thickness
VBBT:	Variable Body Biasing Technique
V_{bs}:	Body bias voltage
V_{ds}:	Drain-to-Source voltage
V_{fb}:	Flat band voltage
V_{gs}:	Gate-to-Source voltage
VLSI:	Very Large Scale Integration
V_{ox}:	Voltage drop across the oxide
V_T:	Thermal voltage
V_{th}:	Threshold voltage
V_{tho}:	Zero-bias voltage
W:	Transistor effective Channel width
γ:	Linearized body effect coefficient
ϕ:	Surface to drain barrier height

ϕ_{ox}:	Oxide tunneling barrier height
φ_s:	Surface-inversion potential
ω_d:	Depletion width under the channel
ε_{ox}:	Dielectric constant of Oxide
ε_{si}:	Dielectric constant of Silicon
μ_o:	Carrier mobility

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CHAPTER ONE

INTRODUCTION

1.1 Background

The increasing prominence of portable systems and the need to limit power consumption in Very Large Scale Integration (VLSI) chips has led to rapid and innovative developments of low power devices in recent years. The increasing need of mobile communication represented by the mobile telephone has been showing remarkable growth. This market has been making tough demands for semiconductor Integrated Circuits (ICs) that consume less power, have higher integration, have multi-function capability and are faster.

To achieve higher density, improved performance and lower power consumption, MOS devices have been scaled for more than 30 years (Dutta, 2016). As a result, transistor delay times decrease by more than 30% per technology generation, resulting in doubling of microprocessor performance every two years (Borkar, 1999). Moore's law which states that: "The number of transistors on a chip doubles every 18 months" (Moore, 1965), has been held true for the last 40 years due to rapid progress and scaling (increased integration on a small surface area) of bulk Complementary Metal Oxide Semiconductor (CMOS) transistor technology. This motivates the need for CMOS scaling in the design of low power circuits in scaled technologies (that is, device feature sizes < 100 nm.) to meet low voltage and low power requirements. According to Tyagi (2007), effective channel length, L and gate oxide thickness, t_{ox} of 35nm and 1.2nm respectively have been demonstrated in

the 65nm technology mode. This, however, cannot go beyond the limit, effective channel length $L \leq$ 10nm, which is subject to quantum mechanical tunneling effects which can initiate a damage leading to reliability concerns of the device. Consequently, there are increasing technology and design problems to be solved if Moore's law has to hold. These limitations include standby power leakage, Short Channel Effects (SCEs), parasitic capacitance issues and interconnect issues.

1.2 Problem Statement

With the substantial growth in portable computing and wireless communication in the last five decades, reduction of power dissipation has become a critical issue. Problems of heat removal or cooling are worsening because the magnitude of power dissipated per unit area is growing with the increased integration of more components on a smaller surface area of a chip.

As a result of continued increased integration of more components on a smaller surface area of a chip, the supply voltage, V_{dd}, has been scaled down in order to keep the power consumption under control. Hence the transistor threshold voltage, V_{th}, has to be commensurately scaled to maintain a high drive current and achieve performance improvement. However, threshold voltage down-scaling results in an exponential increase in the off-state leakage current known as the subthreshold leakage current, I_{sub}. This becomes a limiting factor for further down-scaling of the threshold voltage since it determines the power consumption of a chip in its idle state.

This research is intended to model a Silicon-based CMOS transistor with reduced OFF-state subthreshold leakage current, I_{sub} by varying the threshold voltage, V_{th}, the channel length, L and the device width, W.

1.3 Objectives:

1.3.1 General Objective

The general objective of this research is to obtain a simplified expression for the off-state subthreshold leakage current of a CMOS device and study the effects of the threshold voltage and device dimensions on it using MATHCAD.

1.3.2 Specific Objectives

The specific objectives of this research are:

i) To model the OFF-state subthreshold leakage current, I_{sub} (OFF).

ii) To determine the effect of the threshold voltage, V_{th} on the OFF-state subthreshold leakage current, I_{sub} (OFF).

iii) To determine the effect of transistor channel width, W, on the OFF-state subthreshold leakage current, I_{sub} (OFF).

iv) To determine the effect of transistor effective channel length, L, on the OFF-state subthreshold leakage current, I_{sub} (OFF).

v) To optimize the OFF-state subthreshold leakage current, I_{sub} (OFF).

1.4 Justification

Reduction of CMOS device dimensions, by scaling, to accommodate more components on a chip improves performance, increases transistor density, increases transistor switching speed and reduces power consumption. Transistor delay times decrease by more than 30% per technology generation, resulting in doubling of microprocessor performance every two years. Since switching power is proportional to the square of the supply voltage, (V_{dd}^2), new processes are tailored towards the reduction of supply voltages. This decrease in V_{dd} slows down VLSI devices such as logic gates, thus the threshold voltage, V_{th}, must be lowered to maintain performance. However, continued reduction in the threshold voltage, V_{th}, results in an exponential increase in the sub-threshold leakage current, I_{sub}. Consider an example of a cell phone chip containing one hundred million transistors; if I_{sub} (OFF) is a modest 100nA per transistor, the chip would consume so much standby current (10A) that the battery would be drained in minutes without receiving or transmitting any calls. A desktop Personal Computer chip may be able to tolerate this static power but not much more before facing expensive problems with cooling the chip and the system.

It has also been shown that the OFF-state subthreshold leakage current, I_{sub} (OFF), has increased by about five times per technological generation, for the last three generations. This has been due to the aggressive reduction of device size so that millions of devices can be integrated on a smaller chip area. This will adversely affect most low power devices (microelectronic systems) which usually operate primarily in bursts of activity amid significant periods of inactivity. Standby

subthreshold leakage current reduction can reduce the power dissipation of such devices during these standby periods.

CHAPTER TWO

THEORY AND LITERATURE REVIEW

2.1 Introduction

This chapter discusses the physics of semiconductor devices relevant to the construction, and the basic characteristics of the Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) and the Complementary Metal Oxide Semiconductor (CMOS) transistors. It also looks at the latest literature on the subject area. An insight into the MOSFET as one of the most important electronic devices and its strength that makes it a popular device for Very Large Scale Integration (VLSI) is discussed. MOSFET conduction is discussed based on three different inversion regimes: weak (or subthreshold), moderate and strong inversion. Various subthreshold leakage current mechanisms and models presented during the last two decades are also highlighted.

2.2 The MOSFET Fundamentals

The metal-oxide semiconductor (MOS) transistor has emerged as the most important electronic device, superseding the bipolar junction transistor in sales volume and applications. Its strength derives from its simple structure, low power consumption, especially under steady state direct current (d-c) condition, and low fabrication cost. For these reasons, the MOS transistor continues to be the most popular device for Very Large Scale Integration (VLSI).

The MOS transistor is a four terminal device in which the lateral current flow is controlled by an externally applied vertical electric field (Yang, 1988). A typical MOS transistor, and some of its important features, is shown in Figure 2.1, where

the four terminals are designated as the Source(s), Gate (g), Drain (d) and Substrate (Bulk, b). However, in most simplified analyses, the effect of the substrate is neglected and the MOS transistor is considered as a three-terminal device.

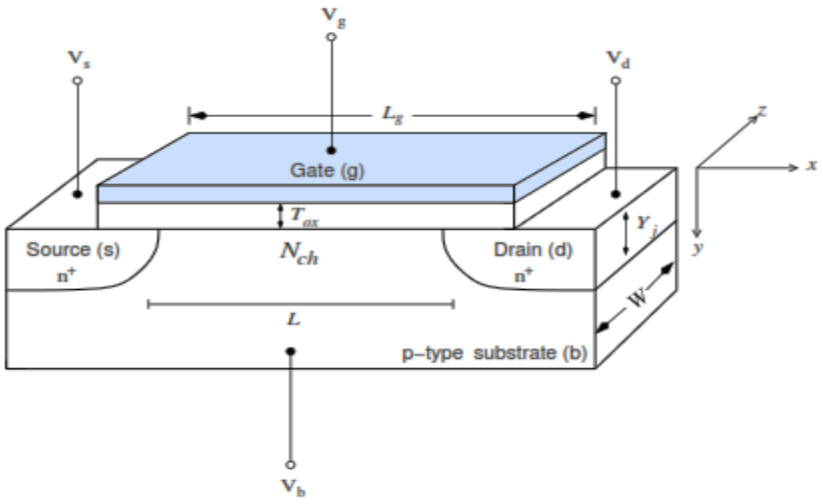


Figure 2.1: Important MOSFET parameters (NMOS) (Butzen, *et.al.*, 2007).

In earlier fabrications of MOSFETs, the gate electrode consisted of a metal such as Aluminium, a silicon-oxide gate dielectric and the silicon substrate. Nowadays the metal gate electrode and silicon oxide based gate dielectric have been replaced by polycrystalline silicon and high-K material (Gate dielectric material with higher permittivity) such as Hafnium Oxide (HfO_2) due to its excellent thermodynamic stability on Silicon as well as sufficient conduction and valence band offsets with Silicon (Chan, 2004, Dutta, 2016). There are several important parameters which determine the characteristics of MOSFETs:

i. Oxide capacitance, C_{ox} is the capacitance per unit area between the gate metal and the bulk or substrate surface.

ii. Gate-source voltage, V_{gs}, is the voltage that is applied between the gate and source to control the operation of the transistor.

iii. Drain-source voltage, V_{ds}, is the voltage which is applied between drain and source.

iv. Threshold voltage, V_{th}, is the minimum voltage that will induce inversion layer which turns on the transistor.

v. Drain-Source current, I_{ds}, is the current that flows between drain and source through the inversion channel induced beneath the gate when the transistor is turned on.

vi. Oxide layer of thickness, t_{ox} which separates the gate and the channel.

The source and the drain are formed by adding impurity dopant into the substrate. The semiconductor material in the source and drain regions is doped with a different type of material from that in the substrate. For example, if the substrate is doped using a trivalent atom such as Boron, the source and drain will be doped using a pentavalent atom such as Arsenic. In this case, an n-channel MOSFET (n-MOSFET or NMOS) will be realized. If the doping process described in the preceding example is reversed, a p-channel MOSFET (p-MOSFET or PMOS) will be realized.

With no voltage applied to the gate, the two back-to-back p-n junctions between the drain and source prevent current flow in either direction. This is true if the channel length is sufficiently long. When a positive voltage is applied to the gate with respect to the substrate, mobile negative charge is induced in the semiconductor below the semiconductor-oxide interface. The negative carriers provide a conduction channel between the source and the drain. Since the current is controlled by the vertical as well as the lateral electric field, this device is also known as the Insulated Gate Field Effect Transistor (IGFET) (Yang, 1988).

The area between the source and drain beneath the gate, the channel, has a length of L and width W. It is where the inversion layer is formed when sufficient voltage is biased to the gate and drain which then turn on the MOSFET. The oxide layer with a certain thickness, t_{ox}, separates the gate and the channel.

Basically, three different inversion regimes can be defined for the operation of the MOS transistor. Based on the inversion conditions of the channel, these regimes are called the **weak inversion** or **subthreshold**, the **moderate inversion** and **strong inversion** regimes.

In general, two mechanisms are responsible for the current flow in a transistor; drift and diffusion. Under weak inversion, the channel surface potential is almost constant across the channel and the current flow is determined by diffusion of minority carriers due to a lateral concentration gradient. Under strong inversion, there exists a thin layer of minority carriers at the channel surface and a lateral electric field which causes a drift current to flow. The moderate inversion regime is considered a transition region between weak and strong inversion where both current flow mechanisms coincidentally exist (Yang, 1988).

2.3 The CMOS Transistor

The Complementary Metal Oxide Semiconductor (CMOS) is a widely used type of semiconductor technology. The term "CMOS" refers to both a particular style of digital circuitry design and the family of processes used to implement that circuitry on integrated circuits (chips). A CMOS inverter is an ingenious circuit which is built

from a pair of NMOS and PMOS transistors operating as complementary switches as illustrated in Figure 2.2.

The power supplies for CMOS are V_{DD} and V_{SS}, or V_{DD} and Ground (GND) depending on the manufacturer. V_{DD} and V_{SS} are carryovers from conventional MOS circuits and stand for the drain and source supplies respectively. These do not apply directly to CMOS, since both supplies are really source supplies. The outputs of the PMOS and NMOS transistors are complementary such that when the input is low, the output is high, and when the input is high, the output is low. Because of this behavior of input and output, the CMOS circuit's output is the inverse of the input.

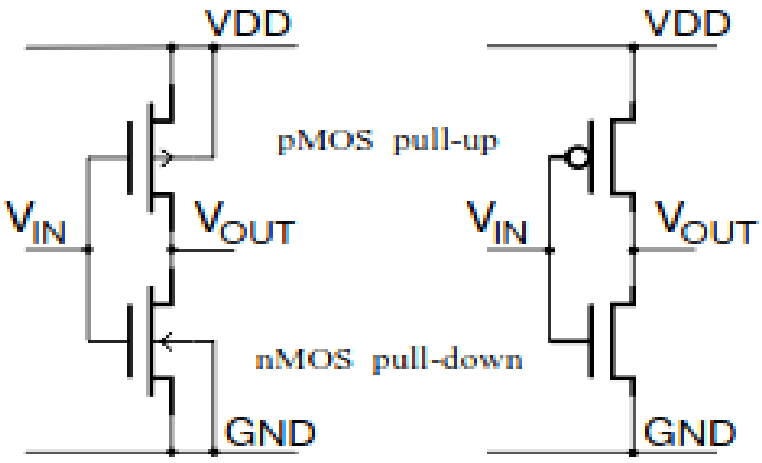


Figure 2.2: Schematic diagrams of a CMOS inverter (Taur, *et.al.*, 1998, Sze, *et.al.*, 2007)

Typical CMOS semiconductors use both NMOS (negative polarity) and PMOS (positive polarity) circuits. Since only one of the circuit types is ON at any given time, CMOS chips require less power than chips using just one type of transistor. This makes them particularly attractive for use in battery-powered devices, such as

portable computers. Personal computers also contain a small amount of battery-powered CMOS memory to hold the date, time, and system setup parameters. Equally, CMOS circuitry dissipates less power than logic families with resistive loads. Since this advantage has increased and grown more important, CMOS processes and variants have come to dominate, thus the vast majority of modern integrated circuit manufacturing is on CMOS processes. As of 2010, Computer Central Processing Units (CPUs), with the best performance per watt each year, have been CMOS static logic since 1976 size (Bohr, 2017).

CMOS circuits use a combination of p-type and n-type Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFETs) to implement logic gates and other digital circuits. Although CMOS logic can be implemented with discrete devices for demonstrations, commercial CMOS products are integrated circuits composed of up to 1.3 billion of transistors of both types, on a rectangular piece of silicon of 82 mm^2 die size (Bohr, 2017).

CMOS circuits are constructed in such a way that all PMOS transistors must have either an input from the voltage source or from another PMOS transistor. Similarly, all NMOS transistors must have either an input from ground or from another NMOS transistor. The composition of a PMOS transistor creates low resistance between its source and drain contacts when a low gate voltage is applied and high resistance when a high gate voltage is applied. On the other hand, the composition of an NMOS transistor creates high resistance between source and drain when a low gate voltage is applied and low resistance when a high gate voltage is applied. CMOS accomplishes current reduction by complementing every n-MOSFET with a p-

MOSFET and connecting both gates and both drains together. A high voltage on the gates will cause the n-MOSFET to conduct and the p-MOSFET not to conduct, while a low voltage on the gates causes the reverse. This arrangement greatly reduces power consumption and heat generation. However, during the switching time, both MOSFETs conduct briefly as the gate voltage goes from one state to another. This induces a brief spike in power consumption and becomes a serious issue at high frequencies.

2.4 Leakage current mechanisms in scaled CMOS devices:

Generally, in nanometer CMOS circuits, the main leakage current mechanisms are gate tunneling, reverse-biased junction band-to-band tunneling (BTBT) and sub-threshold leakage currents, as shown in Figure 2.3.

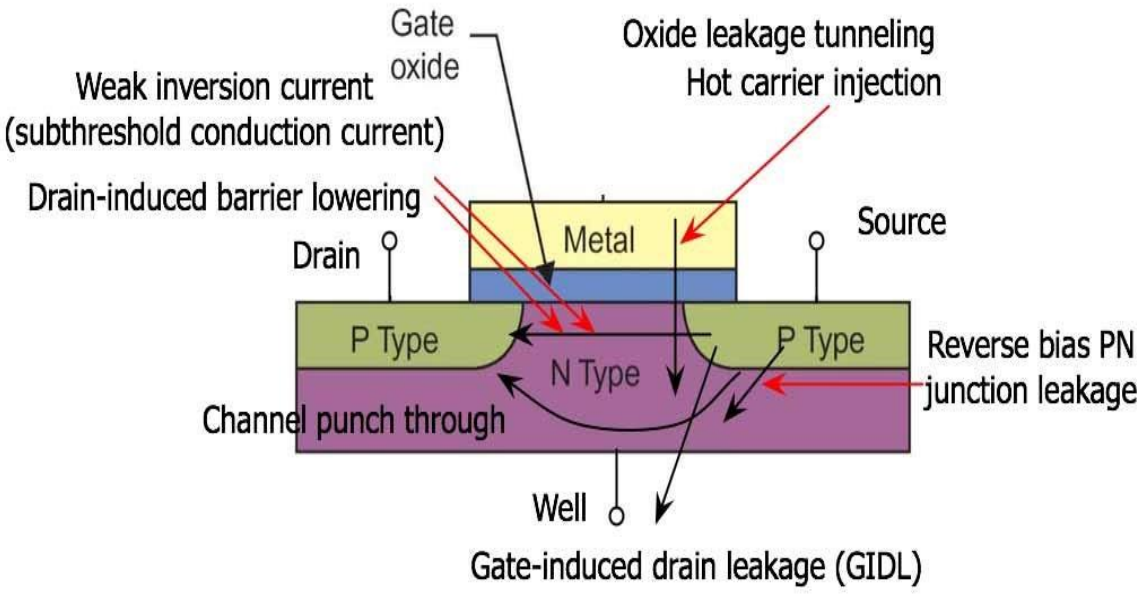


Figure 2.3: Major leakage mechanisms in MOS transistors (Butzen, et.al., 2007).

2.4.1 Gate Oxide Tunneling Current

The aggressive scaling of devices in the nanometer regime increases Short Channel Effects (SCEs) such as Drain Induced Barrier Lowering (DIBL) (cf. appendix) and threshold voltage, V_{th}, roll-off. To control these SCEs, the oxide thickness is made thinner. However, this gives rise to high electric fields resulting in a high direct-tunneling current through the transistor gate insulator (Xu, *et.al.*, 2004).

There are three major gate leakage mechanisms in a MOS structure. The first one is the electron conduction-band (ECB) tunneling, where electrons tunnel from the conduction band of the substrate to the conduction band of the gate (or vice-versa). The second one is the electron valence-band (EVB) tunneling, where electrons tunnel from the valence band of the substrate to the conduction band of the gate. The last one is the hole valence-band (HVB) tunneling, where holes tunnel from the valence band of the substrate to the valence band of the gate (or vice-versa), Figure 2.4.

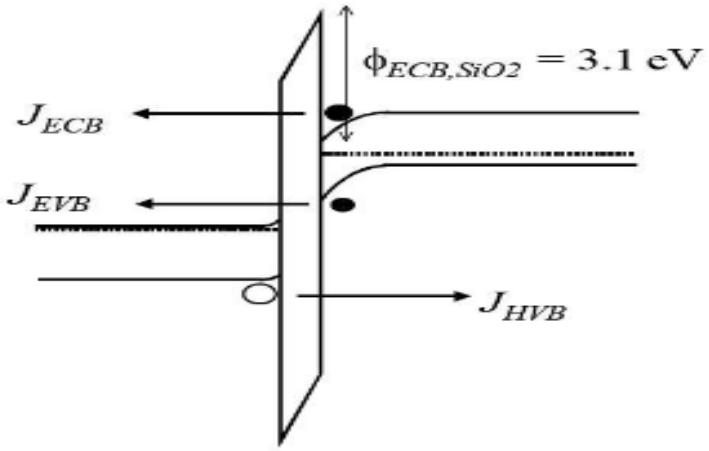


Figure 2. 4: Three mechanisms of gate dielectric tunneling leakage (Cao, 2000).

In figure 2.4, J_{ECB} is the Electron-Conduction Band tunneling current density, J_{EVB} the Electron-Valence Band tunneling current density, J_{HVB} the Hole-Valence-Band tunneling current density and $\phi_{ECB,SiO2}$ is the Electron-Conduction Band gate oxide potential barrier height.

The tunneling of electrons (or holes) from the bulk and source or drain overlap regions through the gate oxide potential barrier into the gate (or vice-versa) is referred to as gate oxide tunneling current. This phenomenon is related with the MOS capacitance concept.

Each mechanism is dominant or important in different regions of operation for NMOS and PMOS transistors. For each mechanism, gate leakage current can be modeled by (Xu, *et.al.*, 2004, Roy, *et.al.*, 2007, Vijayalakshmi, 2017),

$$I_{gate}=W.L.A.\left[\frac{V_{ox}}{t_{ox}}\right]^2 e^{\left[\frac{-B\left[1-\left[1-\frac{V_{ox}}{\phi_{ox}}\right]^{3/2}\right]}{\frac{V_{ox}}{t_{ox}}}\right]} \quad (2.1)$$

where W and L are the effective transistor width and lengths respectively, V_{ox} is the voltage drop across the oxide, t_{ox} is the oxide thickness and ħ is reduced Planck's constant. The parameters A and B in equation (2.1) are defined by,

$$A=\frac{q^3}{16\pi^2\hbar\phi_{ox}} \quad (2.2)$$

and,

$$B=\frac{4\pi\sqrt{2m_{ox}\phi_{ox}^{3/2}}}{3\hbar q} \quad (2.3)$$

where m_{ox} is the effective mass of the tunneling particle, ϕ_{ox} is the tunneling barrier height and q is the electron charge.

2.4.2 Band-To-Band Tunneling (BTBT) Current

The MOS transistor has two p-n junctions; drain and source to well junctions. These junctions are typically reverse biased, causing a p-n junction leakage current. This current is a function of the junction area and doping concentration (Xu, *et.al.*, 2004, Butzen, *et.al.*, 2007). When 'n' and 'p' regions are heavily doped, BTBT leakage dominates the reverse biased p-n junction leakage mechanism.

A high electric field across a reverse-biased p-n junction causes a current flow through the junction due to tunneling of electrons from the valence band of the p-region to the conduction band of the n-region, as illustrated in Figure 2.5.

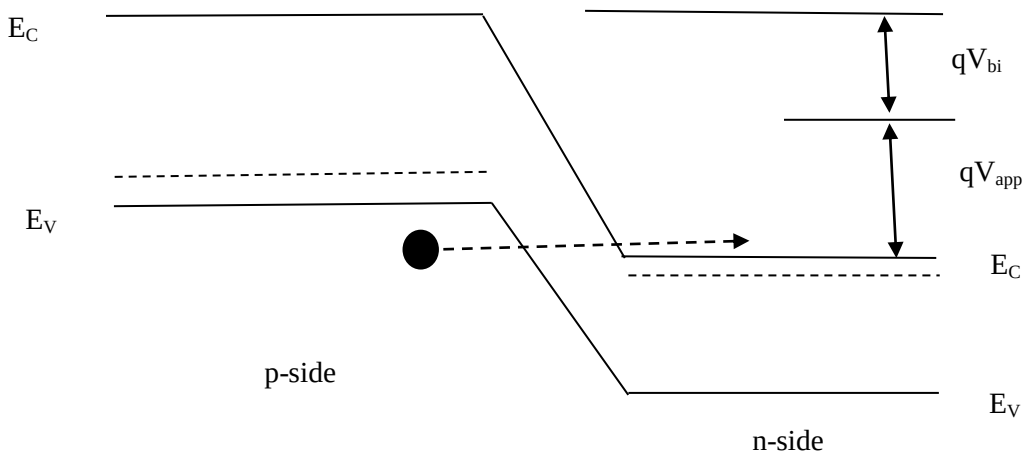


Figure 2.5: BTBT in reverse-biased p-n junction (Vijayalakshmi, 2017).

Tunneling current occurs when the sum of voltage drop across the junction, the applied reverse-bias voltage (V_{app}) and the built-in voltage (V_{bi}) is larger than the

band-gap potential. The tunneling current density through a silicon p-n junction is given by (Roy, *et.al.*, 2007),

$$J_{BTBT} = M.\frac{EV_{app}}{E_g^{1/2}} e^{\left[\frac{-N.E_g^{3/2}}{E}\right]} \quad (2.4)$$

The parameters M and N in equation (2.4) are defined by,

$$M = \frac{\sqrt{2m^* q^3}}{4\pi^3 \hbar^2} \quad (2.5)$$

and,

$$N = \frac{4\sqrt{2m^*}}{3\hbar q} \quad (2.6)$$

where m^* is the effective mass of the electron, E_g is the energy-band gap, V_{app} is the applied reverse-bias and E is the electric field at the junction.

Band-to-Band tunneling leakage, negligible in current processes when compared to the subthreshold and gate oxide leakages, starts to be taken into account in 25nm technologies (Xu, *et.al.*, 2004, Mukhopadhay, 2005). The junction tunneling current depends exponentially on the junction doping and the reverse bias across the junction. Forward body bias can be used to reduce the band-to-band tunneling leakage.

2.4.3 Punchthrough Current

The punchthrough current is the leakage current from the source to the drain via the silicon substrate which is significantly reduced by lowering the temperature. This is

due to the fact that the punchthrough current is mainly due to thermionic emission between the source and the drain.

The punchthrough current, I_p, is given by, (Butzen, *et.al.*, 2007);

$$I_p = I_o e^{\frac{-\Phi}{kT}} \tag{2.7}$$

where Φ is the source-to-drain potential barrier height and the parameter I_o is the current at threshold which is dependent on process and device geometry. It is typically extracted by simulation but can also be calculated from the equation,

$$I_o = \frac{W\mu_o C_{ox} V_T^2 e^{1.8}}{L} \tag{2.8}$$

The $e^{1.8}$ term was found empirically (Sheu, 1987). C_{ox} is the gate oxide capacitance and μ_o is the carrier mobility. The parameter V_T is known as the thermal voltage and is expressed as,

$$V_T = \frac{kT}{q} \tag{2.9}$$

where k is the Boltzmann's constant and T is the absolute temperature.

Thus, the punchthrough current is thermally generated and is strongly reduced at low temperature. This phenomenon is critical in the subthreshold region where the presence of low amplitude leakage currents is easily observable. This feature demonstrates that the operation at low temperature is an effective way to reduce the parasitic punchthrough leakage current in MOSFETs even though their operation is not well optimized at room temperature.

2.4.4 Subthreshold Leakage Current

Subthreshold leakage current, I_{sub}, is defined as the drain-to-source leakage current when the transistor is OFF (Xu, *et.al.*, 2004, Deepaksubramanyan, *et.al.*, 2007, Vijayalakshmi, 2017). It occurs between drain and source when the transistor is operating in the weak inversion region, that is, the gate voltage, V_g, is lower than the threshold voltage, V_{th}; ($V_g < V_{th}$). In this region, supply voltage has been reduced so that the dynamic power consumption is controlled. The minority carrier concentration is almost zero, and the channel has no horizontal electric field, but a small longitudinal electric field appears due to the drain-to-source voltage. In this situation, the carriers move by diffusion between the source and the drain of the MOS transistor. Therefore, the subthreshold leakage current is dominantly due to the diffusion of carriers and it varies exponentially with both the gate-to-source and threshold voltages.

To maintain a high drive current capability, the threshold voltage, V_{th}, has to be reduced too. This, in turn, results in increase in the subthreshold leakage current. This is due to the fact that current does not drop abruptly to zero when $V_{gs} = V_{th}$. Furthermore, the drain current is not zero at zero gate voltage (and large drain voltages), indicating that the gate has lost control of shutting off the device (Yang, 1988). Instead, the current decays off in an exponential fashion when $V_{gs} < V_{th}$. Thus, the output current cannot be turned OFF and the transistor can no longer function as a switch. However, this soft breakdown (exponential current decay) is not seen in long channel devices.

The threshold voltage, V_{th}, for a MOS device is the minimum voltage that will induce inversion layer which turns on the transistor. In order to take into account non-uniform substrate doping, the following standard threshold model (Gu, *et.al.*, 1996) was proposed,

$$V_{th} = V_{fb}+\phi_s+K_1\sqrt{\phi_s-V_{bs}} - K_2[\phi_s-V_{bs}]-\eta V_{ds} \quad (2.10)$$

where ϕ_s is the surface-inversion potential, K_1 and K_2 together model the body effect phenomenon, V_{ds} is the drain-to-source voltage, V_{bs} is the body bias voltage, η is the Drain Induced Barrier Lowering (DIBL) coefficient and V_{fb} is the flat-band voltage. In an idealized MOS structure, it is assumed that the energy-band diagram is flat when the gate voltage is zero. In practice, however, this condition is not realized because of unavoidable work function difference and charges in the oxide and surface states (Yang, 1988). To achieve the flat-band condition for an NMOS, a negative gate voltage is applied to lower the electric field distribution until the charge is reduced to zero at the silicon surface. The gate voltage required to achieve the flat-band condition is known as the flat-band voltage, V_{fb}.

At values of the gate-source voltage, V_{gs} below the threshold voltage, V_{th}, the inversion electron concentration (n_s) is small but nonetheless can allow a small leakage current to flow between the source and the drain, I_{ds}. The differential equation for the surface-inversion potential, φ_s with respect to the gate-source voltage is given by (Mookerjea, 2009),

$$\frac{d\varphi_s}{dV_{gs}} = \frac{C_{ox}}{C_{ox}+C_{dep}} \equiv \frac{1}{n} \qquad (2.11)$$

where φ_s is the surface-inversion potential, C_{ox} is the gate oxide capacitance, C_{dep} is the capacitance of the depletion layer, n is the Subthreshold swing coefficient and V_{gs} is the gate-source voltage

Considering the Berkeley Short-Channel IGFET Model for MOS transistors (BSIM MOS), (Sheu, 1987, Gu, *et.al.,* 1996, Manisha, 2011, Singh, *et.al.,* 2013, Vijayalakshmi, 2017), the subthreshold leakage current for a MOSFET device is expressed by,

$$I_{sub} = I_o . e^{\frac{V_{gs}-V_{th}}{nV_T}} \left[1 - e^{\frac{-V_{ds}}{V_T}}\right] \qquad (2.12)$$

where V_{th} is the threshold voltage, V_{ds} and V_{gs} are drain-to-source and gate-to-source voltages, respectively and n is the subthreshold swing coefficient, for a long channel uniformly doped device given by,

$$n = 1 + \frac{C_b}{C_{ox}} \qquad (2.13)$$

where the parameters C_b and C_{ox} are the bulk (substrate) and the gate oxide capacitances, respectively. These are expressed by equations (2.14) and (2.15) respectively.

$$C_b = \frac{\varepsilon_{si}}{\omega_d} \qquad (2.14)$$

and,

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \qquad (2.15)$$

where ε_{ox} and ε_{si} denote the dielectric constants of the oxide and silicon respectively, ω_d is the depletion width under the channel, and t_{ox} is the gate oxide thickness.

The practical definition of V_{th} in experimental studies is the gate-source voltage V_{gs} at which the drain to source current, I_{ds}, in nano-Amperes (nA) is given by,

$$I_{ds}(nA) = 100 \times \frac{W}{L} \times e^{\frac{q(V_{gs}-V_{th})}{nkT}} \quad (2.16)$$

The 100 value in equation (2.16) is the value of the current at threshold I_o, in nA, and it is derived from,

$$I_o = \frac{W\mu_o C_{ox} V_T^2 e^{1.8}}{L} \quad (2.8)$$

The carrier mobility μ_o is the proportionality constant between the applied electric field (in V/cm) and the resulting velocity of the carriers (in cm/sec). The intrinsic values (for pure silicon) of the mobility for electrons and holes at room temperature (T= 300K) are,

μ_n = 1350cm^2/V·s (for electrons) and μ_p = 480cm^2/V·s (for holes). The fact that holes are more sluggish than electrons has some influence on relative sizes of nMOS and pMOS transistors. The gate-oxide-channel structure forms a capacitor. The gate-oxide capacitance per unit area can be calculated from the equation (2.15), where,

ε_{ox}= 0.351pF/cm is the permittivity (a dielectric constant) of SiO_2. Note that this capacitance is inversely proportional to the thickness of the silicon-dioxide layer. The oxide thickness and the resulting gate capacitance per unit area are parameters specified by the technological process of fabrication of CMOS transistors.

For example, consider a typical 65 nm technology process nMOS transistor at Vgs= 1.0 V, where the gate oxide thickness, $t_{ox,}$ used was 194 nm and V_T^2 at room temperature was 6.76×10^{-6} V^2, (Weste, *et.al*., 2016), then,

$$C_{ox}= \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.51\times10^{-13}}{1.94\times10^{-7}} = 1.81 \times 10^{-6}\mathrm{F/cm^2} \quad (2.17)$$

and,

$$\mu_o C_{ox} V_T^2 e^{1.8} = 1350 \times 1.81 \times 10^{-6} \times 6.76 \times 10^{-6} \times 6.0497 = 9.99\times10^{-8}\ \mathrm{A}$$

$$\approx 100\ \mathrm{nA} \quad (2.18)$$

In practice, this value (2.18) is usually set by CMOS manufacturing Companies, during fabrication, to either 100 nA or 200 nA. The choice of this value by a Company to be 100 nA or 200 nA depends on the carrier mobility, μ_o, the gate oxide capacitance, $C_{ox,}$ the device geometry and the thermal voltage, V_T the Company has adopted for fabrication of the transistor. For lower subthreshold leakage current, I_{sub}, a lower value is desirable, hence the choice of 100 nA in equation (2.16).

The empirical value of the channel length L, is 10 nm; which is the minimum value of L before quantum mechanical tunneling effects set in, while that of the channel width W= 7 nm; which approximates the current design minimum device width, and V_{gs} =0. The current through the device is measured for values of V_{th}= 0 to 300 mV. The 300 mV value approximates the upper edge of the subthreshold region for the CMOS devices (Deepaksubramanyan, *et.al.*, 2007, Weste, *et.al*., 2016).

On a graph of I_{ds} versus Vgs, with logarithmic (base 10) axis for I_{ds}, the subthreshold slope is found as the straight-line approximation of the subthreshold current, normally expressed in units of decades/mV. The Subthreshold swing is the inverse of this slope and is expressed in units of mV/decade. Ideally, it is assumed that the current will drop as fast as possible once $V_{gs}<V_{th.}$ However, in real transistors, current does not abruptly cut off below threshold voltage, but rather drops off exponentially as shown in Figure 2.6,

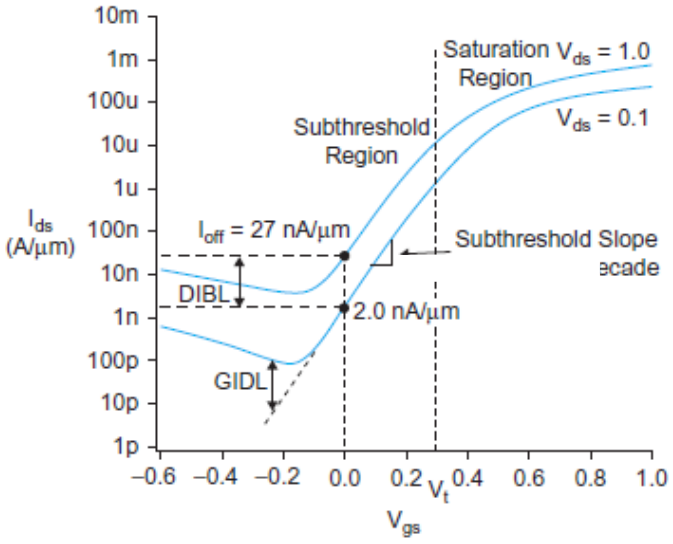


Figure 2.6: I-V characteristics of a 65 nm nMOS transistor at 70°C on a log scale (Weste, *et.al.*, 2016)

When the gate voltage, V_{gs} is high, the transistor is strongly ON. When the gate voltage falls below the threshold voltage, that is $V_{gs}<V_{th}$, the exponential decline in current appears as a straight line on a semi-logarithmic plot of I_{ds} against V_{gs}. The inverse of the slope of this line is known as the subthreshold swing, S, in mV/ decade (Roy, *et.al.*, 2007, Manisha, 2011, Singh, *et.al.*, 2013, Weste, *et.al.*, 2016), given by,

$$S = \left[\frac{d(log_{10}I_{ds})}{dV_{gs}}\right]^{-1} \quad (2.19)$$

This is alternatively defined by,

$$S = n\left[\frac{kT}{q}\right] \ln 10 \quad (2.20)$$

Since $\ln 10 = 2.3$,

$$S = 2.3n\frac{kT}{q} \quad (2.21)$$

Substituting equation (2.13) into equation (2.21) for n, the subthreshold swing, S is found to be,

$$S = 2.3\,\frac{kT}{q}\left[1 + \frac{C_b}{C_{ox}}\right] \quad (2.22)$$

The subthreshold swing describes the exponential behavior of the current as a function of voltage. It also indicates how effectively the transistor can be turned off, that is, the rate of decrease of I_{OFF}, when V_{gs} is decreased below V_{th}. Practically, S can range from 70 to 120 mV/decade for a bulk CMOS process, while the subthreshold swing coefficient, n ranges between 1 and 2 (Deepaksubramanyan, *et.al.*, 2007, Weste, *et.al*., 2016).

As device dimensions and the supply voltage are scaled down to enhance performance, power efficiency and reliability, subthreshold leakage current may limit the scalability of the supply voltage.

2.5 Subthreshold Leakage Current Models:

Several subthreshold leakage current models have been presented during the last two decades. A typical subthreshold leakage model, reported by Narendra, *et.al.* (2006) is given by,

$$I_{sub} = W I_1 . 10^{-\frac{1}{n}(\Delta Vgs + \eta \Delta Vds + \Upsilon \Delta Vbs)} \quad (2.23)$$

where I_1 is the leakage current of a single transistor of unit width in an off- state device with $V_{gs}=V_{bs}=O$ V (zero volts) and $V_{ds}=V_{dd}$. ΔV_{gs}, ΔV_{bs} and ΔV_{ds} are the gate-drive, body bias and drain to source voltages, respectively, reduced based on the above mentioned conditions, η is the Drain- Induced Barrier Lowering (DIBL) coefficient and Υ is the linearized body effect coefficient. Equation (2.23) is obtained having made the assumption that the resulting drain-source Voltage, V_{ds} will be such that,

$$V_{ds} > \frac{3kT}{q} \quad (2.24)$$

Another subthreshold leakage current model was reported by Gu, *et.al.* (1996) and is given by,

$$I_{sub} = I_o . e^{\frac{V_{gs}-V_{th}}{nV_T}} \left[1 - e^{\frac{-V_{ds}}{V_T}}\right] \quad (2.12)$$

Finally, another subthreshold leakage current model was reported by Roy, *et.al.* (2007) is given by,

$$I_{sub} = I_o W e^{\frac{Vgs-(Vtho-\eta Vds-\gamma Vbs)}{nV_T}} \left(1-e^{\frac{-Vds}{V_T}}\right) \quad (2.25)$$

where V_{tho} in equation (2.25) is the zero-bias threshold voltage.

In this thesis, a more simplified model is derived (refer to equation 3.14) which is then analysed to show how transistor features can be varied to obtain a transistor with reduced OFF-state subthreshold leakage current.

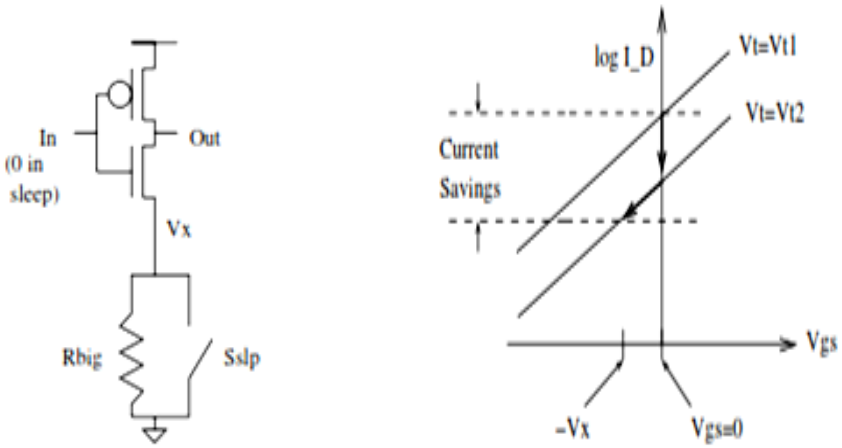
2.6 Some Existing Techniques for Subthreshold Leakage Current reduction:

This section gives a brief highlight of some existing techniques for subthreshold leakage current reduction advanced in the last two decades. Equation (2.12) (Sheu, 1987, Gu, *et.al.*, 1996, Manisha, 2011, Singh, *et.al.*, 2013, Vijayalakshmi, 2017), shows that exponential decreases in the subthreshold leakage current, $I_{sub,}$ are possible by either increasing the threshold voltage, V_{th} or by decreasing V_{gs}. Alternatively, modifying transistor structures, such as by the use of stacks, decreasing V_{gs} in standby mode by raising the source voltage through switched-source-impedance, biasing the body voltage to change V_{th}, using dual-threshold or multi-threshold CMOS techniques, overdriving the gate voltage of sleep devices in active mode, and varying doping levels can be used to respond to the challenge of decreasing Subthreshold Leakage current (Horiguchi, *et.al.*, 1993, Xu, *et.al.*, 2004, Dutta, 2016). Existing techniques for subthreshold leakage reduction explore some of these options.

2.6.1 Switched Source Impedance

One obvious method for reducing leakage current is to decrease V_{gs} in standby mode by raising the source voltage through switched-source-impedance CMOS (Horiguchi, *et.al.*, 1993). In this approach, a passive resistor is switched in between a gate's source nodes and ground during standby mode. During active mode, the resistor is shorted out so that there is no additional delay penalty.

The presence of the resistor in standby mode introduces a positive voltage at V_X due to the leakage current through R_{big} as seen in Figure 2.7a.



(a) (b)

Figure 2.7: Switched-Source-Impedance, (a) Circuit Example, (b) Savings (Horiguchi, *et.al.*, 1993)

The voltage V_X reduces leakage current in two ways. First, the increased source voltage of the NMOS device causes an increase in the threshold voltage due to the well-known equation (2.10) (Sheu, 1987, Manisha, 2011, Singh, *et.al.*, 2013). This higher V_{th} causes a shift in the current-V_{gs} curve in Figure (2.7b) from V_{th}= V_{th1} to

V_{th}= V_{th2}. Furthermore, the increased V_X reduces V_{gs} of the NMOS device, causing the operating point to shift downward along the current-V_{gs} curve. The combination of these two effects lowers the standby leakage current. In practice, switched-source impedance circuits are rare because the resistor must be large and resistor placement depends on knowing the standby state of every gate. Since there is no perfect switch, the resistance of the switch often replaces the explicit resistor for this technique.

2.6.2 Stack Effect

A similar and more practical technique for subthreshold leakage reduction takes advantage of the stack effect. The term *stack effect* refers to the reduction of subthreshold leakage by stacking multiple FETs in series (Xu, *et.al.*, 2004, Saxena, *et.al.*, 2013, Sharma, *et.al.*, 2013). Figure (2.8) shows a case of artificially introducing the stack effect to an inverter, but stacks of transistors occur naturally in many logic gates (*that is*, NAND).

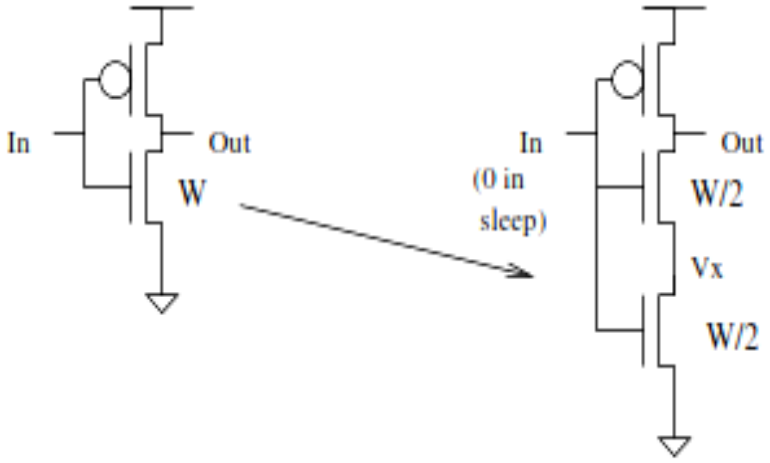


Figure 2.8: Artificial Creation of Stack Effect (Saxena, *et.al.*, 2013).

The stack effect provides leakage reduction in the same way as switched-source-impedance. The last device in the stack essentially appears as impedance to any leakage current, so the voltage V_X becomes non-zero.

At that point, the effects shown in Figure (2.7b) occur as previously described. Notice that the imposed stack effect approach is essentially the switched-source-impedance approach without the resistor. This approach just uses the resistance of the non-ideal switching FET in an OFF state.

Designers take advantage of the stack effect in two ways. First, one can exploit natural stacks in a circuit by determining an input vector at design time that turns off stacks of devices. Several algorithms exist for applying test vectors to a circuit at design time to find the vector that generates the lowest leakage current (Xu, *et.al.,* 2004, Saxena, *et.al.,* 2013). When the circuit enters standby mode, this low-leakage vector is multiplexed into the circuit inputs.

Artificial introduction of stacks to a circuit (Narendra, *et.al.,* 2006) can enhance the gains from the vector-finding method of leakage reduction. In this approach, stacks are introduced to gates off of the critical path (Figure 2.8). While slower itself, the new gate presents the same capacitive load at its input, so it does not slow down previous gates. This method trades off speed on non-critical paths and design time for reduced leakage. A new model for determining the savings, introduced by

forcing stacks, allows designers to determine the usefulness of the approach for a given technology (Narendra, *et.al.,* 2006, Sharma, *et.al.,* 2013).

2.6.3 Body Biasing

An entirely different approach to reducing subthreshold leakage biases the body voltage to change V_{th}. In order to maintain the cut off condition for all the substrate-to-channel junctions, the substrate is usually connected to the most negative power supply in an NMOS circuit (to the most positive in a PMOS circuit). The resulting reverse bias voltage between the source and body will have an effect on device operation. The reverse bias voltage will widen the depletion region. This will in turn reduce the channel depth (Maheshwari, 2014). There are many angles taken to use this technique, such as the Variable Body Biasing Technique (VBBT) (Yadav, *et.al.,* 2015), but they all require isolation of the bulk for different FETs (as in a triple well process).

2.6.4 Dual-Threshold CMOS

Dual-threshold CMOS techniques use FETs having two thresholds to reduce leakage currents. The most straightforward application of dual-threshold CMOS uses all low V_{th} FETs on the critical path and high V_{th} FETs off of the critical path. The high V_{th} devices placed at design time reduce leakage while increasing delay off of the critical path. The placement of these devices can become complicated since the high V_{th} devices can slow down parts of the circuit enough to create new critical paths (Sreenivasulu, 2013).

Nevertheless, several algorithms exist for that purpose that maintains a high supply voltage for gates on the critical path and by using a low supply voltage for the gates

off the critical path (Sundararajan, *et.al.*, 1999). One advantage of dual-threshold CMOS is that the leakage savings occur in both active and standby modes. Disadvantages include more complicated design time and the inability to stop critical path leakage during standby mode.

Dual-threshold CMOS is particularly useful for some special logic styles. For example, domino logic can use high V_{th} devices on the precharge path (Kao, *et.al.*, 2002, Sreenivasulu, 2013). All of the pull-down paths remain fast because of the low V_{th} devices, but each path between the rails contains at least one high V_{th} device. This allows the tradeoff of precharge time with reduced leakage.

2.6.5 Multi-Threshold CMOS (MTCMOS)

Multi-Threshold CMOS (MTCMOS) refers to a circuit technique that uses a high V_{th} footer and/or header FET to sever a circuit from the power rails as illustrated in Figure 2.9 (Mutoh, 1995, Yadav, *et.al.*, 2015).

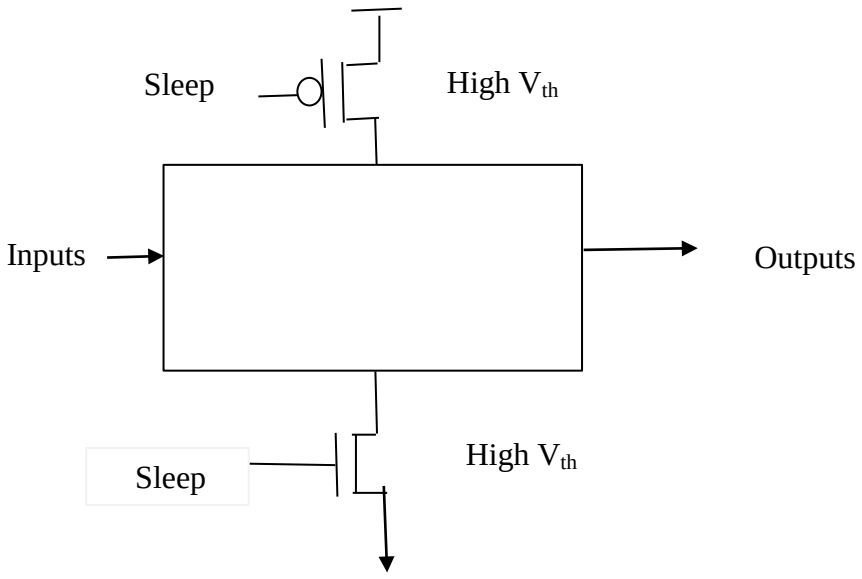


Figure 2.9: MTCMOS Schematic (Kumar, *et.al.*, 2013).

Similar approaches have been applied to caches (Powell, 2001, Anis, *et.al.,* 2003, Kumar, *et.al.,* 2013) and to DRAMs (Sakata, 1994).

In the active mode, the high V_{th} switches are ON to enable regular circuit operation. Turning OFF the high V_{th} devices in standby mode places at least one high V_{th} FET on each path from power to ground, thereby reduces the leakage current significantly. Small sleep devices reduce the leakage current in standby mode but slow down transitions in active mode. The loss of performance occurs because smaller sleep devices sink less current through to ground.

This exacerbates the bouncing created at the virtual rails and effectively pinches V_{ds} for the low V_{th} circuit. Furthermore, this rail bounce depends on the discharge pattern of the circuit, so it can be difficult to predict worst-case performance.

Combinational logic blocks only need a sleep device on one rail, but sequential MTCMOS circuits are more complicated. Simply disconnecting a circuit from the rails in standby destroys any state previously stored in that circuit. Special care is necessary to retain state in MTCMOS sequential circuits. Despite some of the design difficulties, MTCMOS techniques appear to be viable for reducing leakage currents in new technologies.

2.6.6 Boosted Gate MOS (BGMOS) and Super Cut-Off CMOS (SCCMOS)

Two additional proposals for reducing leakage basically increase the effectiveness of MTCMOS sleep transistors. The Boosted Gate MOS (BGMOS) approach (Inukai, 2000) suggests that overdriving the gate voltage of sleep devices in active

mode can reduce the area devoted to sleep devices. The overdriven (above V_{dd}) gate voltage enables a smaller device to sink the required amount of current in active mode while still effectively stemming the leakage current in standby mode. A similar approach called Super Cut-off CMOS (SCCMOS) advocates under-driving gate voltages in standby mode (Kawaguchi, *et.al.*, 2000, Kumar, *et.al.*, 2013). For example, an NMOS sleep device would be turned OFF in standby mode with a negative gate voltage rather than a gate voltage of 0 volts. From equation (2.11), we see that the negative gate voltage provides exponentially decreasing leakage current through the sleep device.

Despite the existence of these techniques, problems of heat removal or cooling, aggravated by increasing subthreshold leakage current, continue worsening because the magnitude of power dissipated per unit area keeps on growing with the increased integration of more components on a smaller surface area of a chip. Some of the techniques, like the use of stacks, results in slower switching speeds for the devices making it unsuitable for use in devices where high switching speed is required.

CHAPTER THREE

METHODOLOGY

3.1 Introduction

In this chapter, the expression used to examine the effect of varying the threshold voltage, V_{th}, the transistor's channel width, W and its effective length, L on off-state the subthreshold leakage current, I_{sub} (OFF) was derived. The obtained expression was then evaluated using MATHCAD.

3.2 Derivation of the simulation equation

In a practical CMOS transistor, the drain-source current, I_{ds} is exponentially proportional to the surface inversion potential, φ_s, that is,

$$I_{ds} \propto e^{\frac{q\varphi_S}{kT}} \qquad (3.1)$$

Now, the derivative of the surface inversion potential, φ_s, against the gate to source voltage, V_{gs} is given by,

$$\frac{d\varphi_S}{dV_{gs}} = \frac{C_{ox}}{C_{ox}+C_{dep}} \equiv \frac{1}{n} \qquad (2.11)$$

Rewriting equation (2.11) implies that,

$$n = 1 + \frac{C_{dep}}{C_{ox}} \qquad (3.2)$$

where C_{dep} is the capacitance of the depletion layer.

Integrating equation (2.11), that is,

$$\int d\varphi_s = \frac{1}{n}\int dV_{gs} \tag{3.3}$$

or,

$$\varphi_s = constant + \frac{V_{gs}}{n} \tag{3.4}$$

where the constant parameter in equation (3.4), is,

$$constant = \frac{-V_{th}}{n} \tag{3.5}$$

then by using equations (3.4) and (3.5) in the index of the exponential of proportionality (3.1), results in,

$$\propto \quad e^{q\left(\frac{-V_{th}}{n}+\frac{V_{gs}}{n}\right)/kT} \tag{3.6}$$

and,

$$I_{ds} = I_o\ e^{q\left(\frac{-V_{th}}{n}+\frac{V_{gs}}{n}\right)/kT} \tag{3.7}$$

where,

$$I_o = \frac{W\mu_o C_{ox} V_T^2 e^{\frac{qV_{gs}}{nkT}}}{L}\left(1-e^{\frac{-V_{ds}}{V_T}}\right) \tag{3.8}$$

Using equations (2.9) and (2.20), equation (3.8) simplifies to,

$$I_o = \frac{W\mu_o C_{ox} V_T^2 e^{\frac{V_{gsln10}}{S}}}{L}\left(1-e^{\frac{-V_{ds}}{V_T}}\right) \quad (3.9)$$

Now, at threshold,

$$I_o = \frac{W\mu_o C_{ox} V_T^2 e^{1.8}}{L} \quad (2.8)$$

When evaluated gives (refer to results 2.17 and 2.18),

$$I_o = \frac{100\,W}{L} \quad (3.10)$$

Now, from equations (2.8), (2.9) and (3.7),

$$I_{ds} = I_o\, e^{\left(\frac{(V_{gs} - V_{th})\ln 10}{S}\right)} \quad (3.11)$$

When the CMOS device is in standby mode the leakage current, I_{ds}, is also referred to as the subthreshold leakage current, I_{sub} (also denoted as I_{OFF}). In this OFF-state, V_{gs} =0, thus equation (3.11) is rewritten as,

$$I_{sub} = I_o\, e^{\left(\frac{-V_{th}\ln 10}{S}\right)} \quad (3.12)$$

This simplifies to,

$$I_{sub} = I_o \times 10^{\frac{-V_{th}}{S}} \quad (3.13)$$

Thus by using equations (3.10) and (3.13),

$$I_{sub} = 100 \times \frac{W}{L} \times 10^{\frac{(-V_{th})}{s}} \quad (3.14)$$

Thus, the characteristics of subthreshold leakage current in the OFF state, I_{sub} (in nA) when the threshold voltage, V_{th} and device dimensions (channel length, L and width, W) are varied, can be determined by the model equation (3.14).

CHAPTER FOUR

RESULTS AND DISCUSSIONS

4.1 Introduction

In this chapter, the results obtained from modelling a CMOS device based on the variations in the threshold voltage, V_{th}, transistor effective width, W and the transistor's effective channel length, L and their effects on the value of the OFF-state subthreshold leakage current, I_{sub} are discussed and presented. The model equation (3.13) is analyzed by varying the subthreshold swing, S through three different sets of values.

4.2 Effect of threshold voltage, V_{th} on the OFF-state subthreshold leakage current, I_{sub}

The subthreshold swing, S in equation (3.14) is varied through S= 60, 90 and 120 mV/decade while the values of W and L are set at 7 nm and 10 nm respectively. Substituting the values of S, W and L respectively, into the model equation (3.14), three equations (4.1a), (4.1b) and (4.1c) are obtained.

$$I_{sub1}(OFF)(A) = 100 \times 7.0 \times 10^{-10} \times 10^{\frac{-V_{th}}{60}} \quad (4.1a)$$

$$I_{sub2}(OFF)(A) = 100 \times 7.0 \times 10^{-10} \times 10^{\frac{-V_{th}}{90}} \quad (4.1b)$$

$$I_{sub3}(OFF)(A) = 100 \times 7.0 \times 10^{-10} \times 10^{\frac{-V_{th}}{120}} \quad (4.1c)$$

In the MATHCAD worksheet, the variable(s) and the function that depends on the behaviour of the variables are initially defined by entering,

V_{th}:0;300 (4.1d)

Input (4.1d) defines the range of V_{th} over which $I_{sub}(A)$ is passing through the device. The leakage current I_{sub} is a function of V_{th}, and it is defined from equations (4.1a), (4.1b) and (4.1c) as,

$$I_{sub1}(V_{th}): 100 * 7.0 * 10^{-10} * 10\text{^} - V_{th}/60 \quad (4.1e)$$

$$I_{sub2}(V_{th}): 100 * 7.0 * 10^{-10} * 10\text{^} - V_{th}/90 \quad (4.1f)$$

$$I_{sub3}(V_{th}): 100 * 7.0 * 10^{-10} * 10\text{^} - V_{th}/120 \quad (4.1g)$$

The data and its graph were obtained by inputting the commands,

V_{th}= $I_{sub1}(V_{th})$ = $I_{sub2}(V_{th})$ = and $I_{sub3}(V_{th})$ = (4.1h)

Figure 4.1 shows plots of the data obtained from equations (4.1e), (4.1f) and (4.1g) where the leakage current, I_{sub} is plotted against the threshold voltage, V_{th} for different values of the subthreshold swing, S.

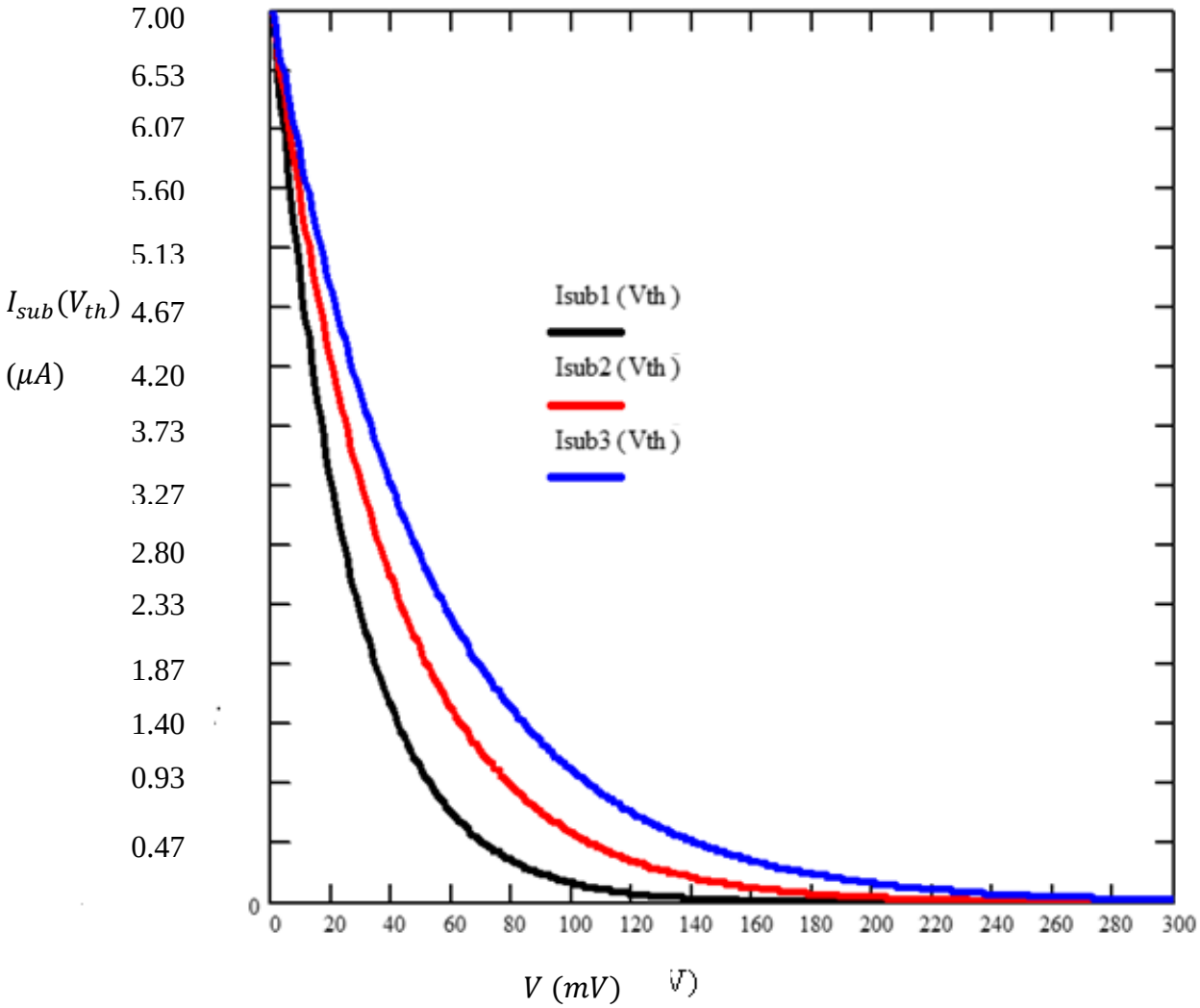


Figure 4.1: Variation of I_{sub} with V_{th}.

These graphs show that the leakage current, I_{sub} decreases exponentially with increase in the threshold voltage, V_{th}. The graphs also show that for a scaled CMOS device, whose channel length, L= 10 nm, the channel width, W= 7 nm, V_{gs} =0 (OFF-state) and the subthreshold swing, S= 60 mV/decade, the threshold voltage, V_{th} that results in zero OFF-state subthreshold leakage current, $I_{sub}\ (OFF)$, is about 140 mV. Increasing the subthreshold swing, S to 90 mV/decade increases the threshold

voltage, V_{th} for zero OFF-state subthreshold leakage current, $I_{sub}\ (OFF)$ to about 180 mV. Further increment of the subthreshold swing, S to 120 mV/decade proportionally increases the threshold voltage, V_{th} for zero OFF-state subthreshold leakage current, $I_{sub}\ (OFF)$ to about 240 mV.

Thus, for minimum leakage current, low values of the threshold voltage, V_{th} = 140 mV and subthreshold swing, S of 60 mV/decade, are desirable.

From these observations, it can be concluded that, for given W and L, three options can be adopted as ways of minimizing I_{sub}. These include;

i) Choosing a large V_{th}. This is, however, not desirable since a large V_{th} reduces the ON-current (I_{on}) and therefore increases the gate delays.
ii) Reducing the subthreshold swing, S by using a lower value of n. This can be achieved by increasing the gate oxide capacitance, C_{ox}, that is, by using a thinner gate oxide material, and decreasing the capacitance of the depletion layer, C_{dep}, the latter being achieved by increasing W.
iii) Additionally, the transistor is operated at a lower temperature. Low operational temperature results in a low subthreshold slope factor, S as shown by equation (2.20). This last approach is valid in principle but rarely used because cooling adds considerable costs.

4.3 Effect of Channel width, W on the OFF-state subthreshold leakage current, I_{sub}

The current through the device is measured for values of W ranging from 7 nm to 32 nm while the subthreshold swing, S in equation (3.14) is varied through S= 60, 90

and 120 mV/decade. The values of V_{th} and L are set at 300 mV and 10 nm respectively.

Substituting these values of S, L and V_{th} in the model equation (3.14) results in equations (4.2a), (4.2b) and (4.2c).

$$I_{sub1}(OFF)(A) = 100 \times \frac{W}{10} \times 10^{-9} \times 10^{\frac{-300}{60}} \qquad (4.2a)$$

$$I_{sub2}(OFF)(A) = 100 \times \frac{W}{10} \times 10^{-9} \times 10^{\frac{-300}{90}} \qquad (4.2b)$$

$$I_{sub3}(OFF)(A) = 100 \times \frac{W}{10} \times 10^{-9} \times 10^{\frac{-300}{120}} \qquad (4.2c)$$

In the MATHCAD worksheet, the variable(s) and the function that depends on the behaviour of the variable are initially defined by entering,

W:7;32 (4.2d)

Equations (4.2a), (4.2b), (4.2c) and (4.2d) define the ranges of W and S over which $I_{sub}(A)$ is passing through the device for different values of the subthreshold swing, S. The leakage current I_{sub} is a function of W, and it can be simplified from equations (4.2a), (4.2b) and (4.2c), together with the constant parameters in the model equation, and defined as,

$$I_{sub1}(W): 100 * \frac{W}{10} * 10^{-9} * 10^{\frac{-300}{60}} \qquad (4.2e)$$

$$I_{sub2}(W): 100 * \frac{W}{10} * 10^{-9} * 10^{\frac{-300}{90}} \qquad (4.2f)$$

$$I_{sub3}(W): 100 * \frac{W}{10} * 10^{-9} * 10^{\frac{-300}{120}} \qquad (4.2g)$$

The data and its graphs were obtained by entering the commands,

W= $I_{sub1}(W) =$ $I_{sub2}(W) =$ and $I_{sub3}(W) =$ (4.2h)

Figure 4.2 shows plots of the data obtained from equations (4.2e), (4.2f) and (4.2g) where the OFF-state subthreshold leakage current, I_{sub} is plotted against the device's channel width, W, for different values of the subthreshold swing, S.

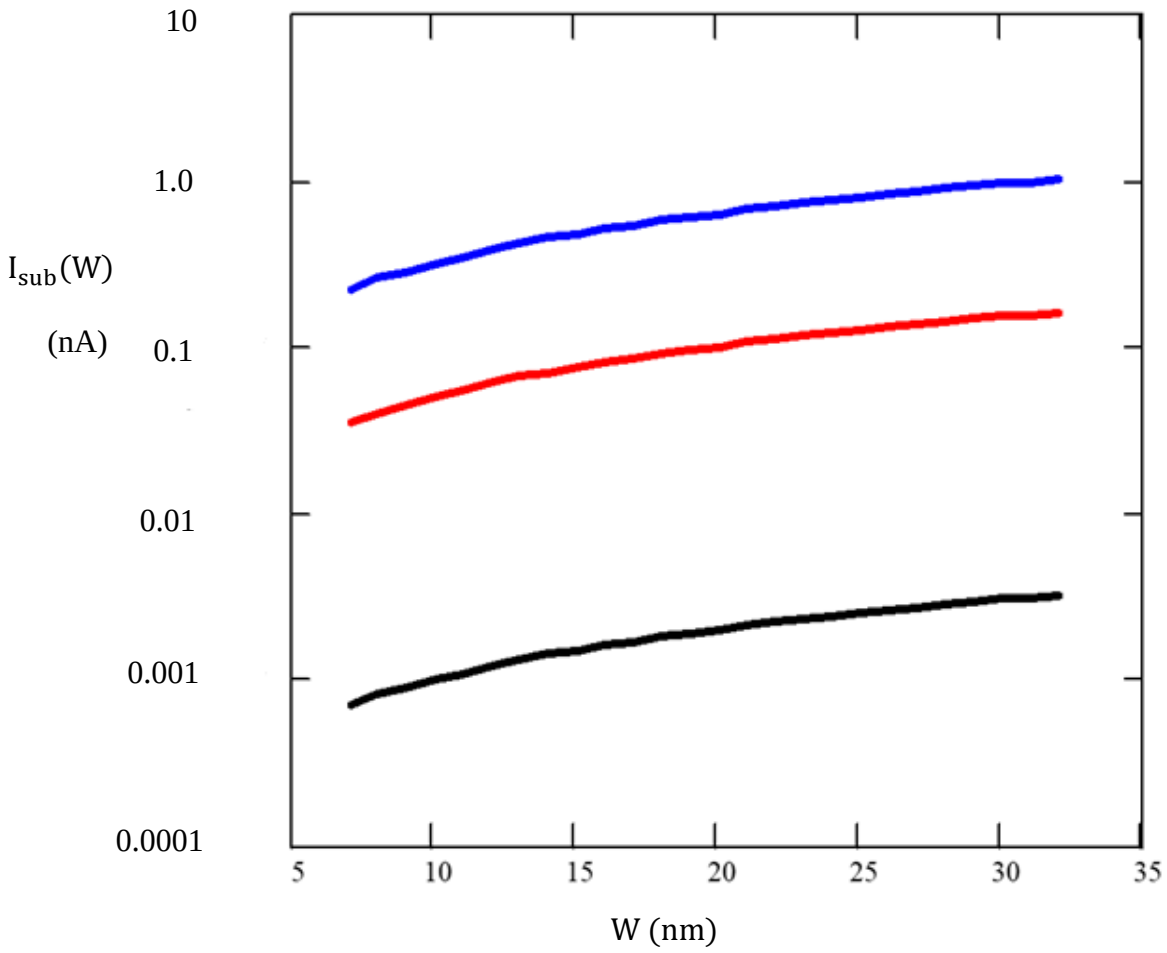


Figure 4.2: Variation of Isub with W

The graphs show that the OFF-state subthreshold leakage current, I_{sub}, increases almost linearly with increase in the channel width, W, on first approximation. It can

also be seen that when the subthreshold swing, S= 60 mV/decade, the OFF-state subthreshold leakage current, I_{sub} increases almost linearly from an approximate minimum of 1.0 pA to a maximum value of about 50 pA. When the subthreshold swing, S= 90 mV/decade, the OFF-state subthreshold leakage current, I_{sub} increases almost linearly from an approximate minimum value of 500 pA to a maximum value of about 0.1 nA. When the subthreshold swing, S was further increased to 120 mV/decade, the OFF-state subthreshold leakage current, I_{sub} increased almost linearly from an approximate minimum value of 0.5 nA to a maximum value of about 1.0 nA.

Thus, for minimum leakage current, low values of W = 7 nm and the subthreshold swing, S of 60 mV/decade, are desirable.

The graphs also show that for a Silicon-based CMOS device, of minimum length, L= 10 nm and V_{gs} =0 (OFF-state), whose threshold voltage, V_{th} has been set at 300 mV and with a subthreshold swing, S of 60 mV/decade, the channel width, W, should be about 7 nm for minimal I_{sub}. ($I_{sub} \approx 0.8$ pA).

This is because if the channel width, W increases, the carrier density of the device also increases. This results in more carriers tunneling across the source-drain channel below the gate, hence increasing I_{sub}. The subthreshold swing, S indicates how much the gate voltage, V_{gs} must drop to decrease the leakage current by an order of magnitude. Thus, an increase in the subthreshold swing, S also causes an increase in the OFF-state subthreshold leakage current, I_{sub}.

4.4 Effect of Channel length, L on the OFF-state subthreshold leakage current, I_{sub}

For the simulation process, the subthreshold swing, S is varied through three different values of S= 60, 90 and 120 mV/decade. The current through the device is measured over this range of S, for the empirical value of V_{th} of 300 mV and L ranging from 10 nm to 28 nm, respectively.

Substituting these values of S, W and V_{th} in the model equation (3.14) results in equations (4.3a), (4.3b) and (4.3c),

$$I_{sub1}(OFF)(A) = 100 \times \frac{7}{L} \times 10^{-9} \times 10^{\frac{-300}{60}} \quad (4.3a)$$

$$I_{sub2}(OFF)(A) = 100 \times \frac{7}{L} \times 10^{-9} \times 10^{\frac{-300}{90}} \quad (4.3b)$$

$$I_{sub3}(OFF)(A) = 100 \times \frac{7}{L} \times 10^{-9} \times 10^{\frac{-300}{120}} \quad (4.3c)$$

In the MATHCAD worksheet, the variable(s) and the function that depends on the behaviour of the variable are initially defined by typing;

L:10;28 (4.3d)

Equation (4.3d) defines the range of L over which $I_{sub}(A)$ is passing through the device. The leakage current I_{sub} is a function of L, and it is simplified from equations (4.3a), (4.3b) and (4.3c), together with the constant parameters in the simulation equations, and defined as,

$$I_{sub1}(L): 100 * \frac{7}{L} * 10\text{^} - 9 * 10\text{^} \frac{-300}{60} \quad (4.3e)$$

$$I_{sub2}(L): 100 * \frac{7}{L} * 10\text{^} - 9 * 10\text{^} \frac{-300}{90} \quad (4.3f)$$

$$I_{sub3}(L): 100 * \frac{7}{L} * 10\text{^} - 9 * 10\text{^} \frac{-300}{120} \quad (4.3g)$$

The data and its graphs were obtained by entering the commands,

L= $I_{sub1}(L)$ = $I_{sub2}(L)$ = and $I_{sub3}(L)$ = (4.3h)

Figure 4.3 shows plots of the data obtained from equations (4.3e), (4.3f) and (4.3g) where the OFF-state subthreshold leakage current, I_{sub} is plotted against the channel length, L for the range of values of the subthreshold swing, S.

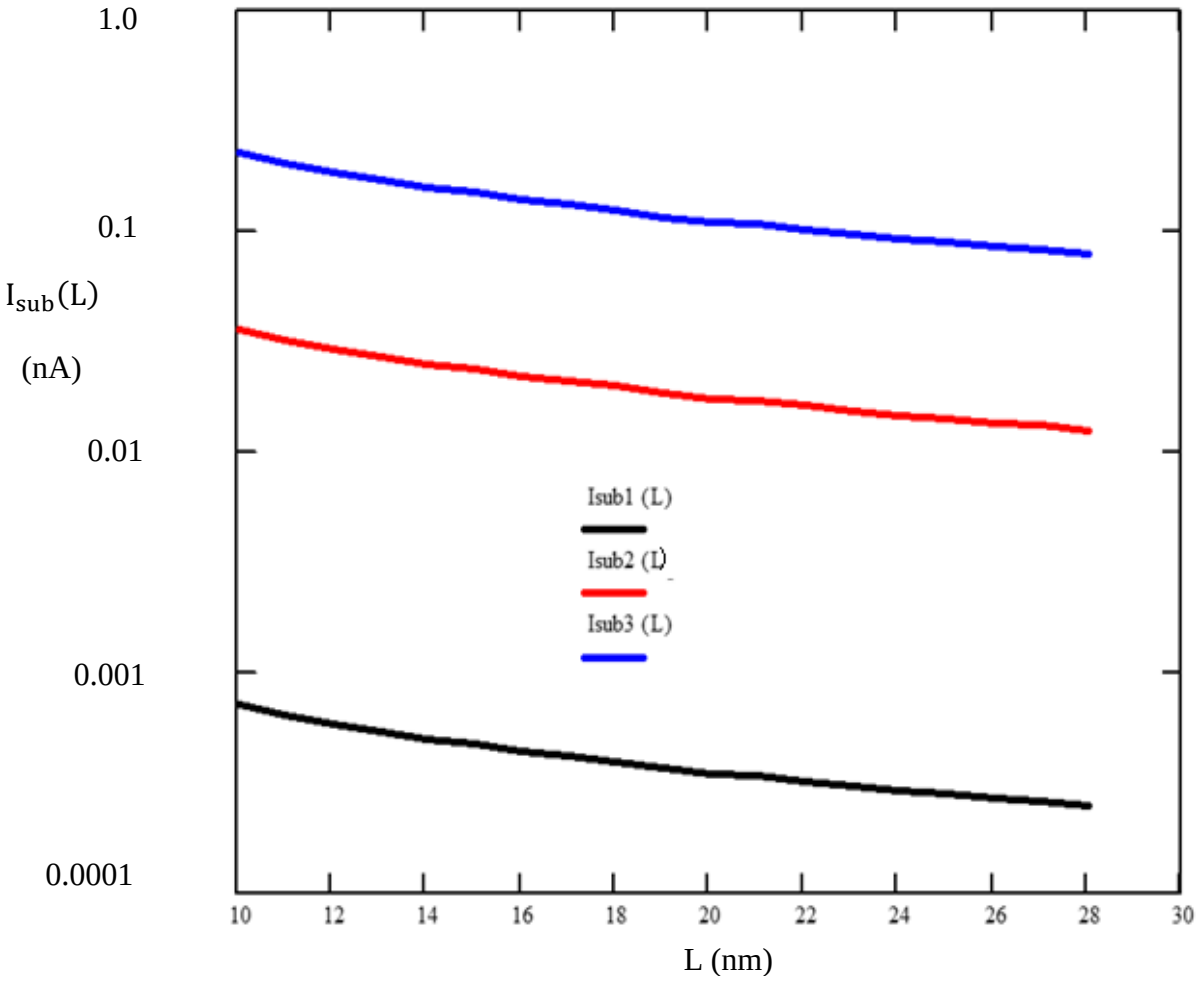


Figure 4.3: Variation of Isub with L.

The graphs show that the OFF-state subthreshold leakage current, I_{sub} (OFF) decreases almost linearly on first approximation with increase in the effective channel length, L of a Silicon-based CMOS transistor. The graphs also show that when the subthreshold swing, S= 60 mV/decade, the OFF-state subthreshold leakage current, I_{sub} decreases almost linearly from an approximate maximum of 8.0 pA to a minimum value of about 5.0 pA. When the subthreshold swing, S= 90 mV/decade, the OFF-state subthreshold leakage current, I_{sub} decreases almost linearly from an approximate maximum value of 50 pA to a minimum value of about 10 pA. When the subthreshold swing, S was further increased to 120 mV/decade, the OFF-state subthreshold leakage current, I_{sub} decreased almost linearly from an approximate maximum value of 0.5 nA to an approximate minimum value of about 0.1 nA. It can also be seen that, the OFF-state subthreshold leakage current, I_{sub} was much higher when S was raised to 90 and 120 mV/decade than when S was set at 60 mV/decade, shown by the wider gap between the former ranges of S and the latter.

Thus, for minimum leakage current, a high value of L= 28 nm and a low value of the subthreshold swing, S of 60 mV/decade, are desirable.

The graphs also show that for a Silicon-based CMOS device, of channel width, W= 7 nm and V_{gs} =0 (off-state), whose threshold voltage, V_{th} has been scaled to 300 mV and with a subthreshold swing, S of 60 mV/decade, the effective channel length should be about, L= 28 nm for minimal I_{sub}. ($I_{sub} \approx 0.5\ pA$).

4.5 Summary

The optimization of the OFF-state subthreshold leakage current in sub sections 4.2, 4.3 and 4.4, indicates that the values of L and W should be 20 nm and 7nm, respectively, while the threshold voltage should be scaled to V_{th}= 140 mV. The value of the subthreshold swing is 60 mV/decade.

Given that the subthreshold slope factor S is 60 mV/decade and the values of the transistor effective channel length, L is 28 nm, its channel width, W is 7 nm and the threshold voltage, V_{th} is 140 mV, then by equation (3.13), the value of the OFF-state subthreshold leakage current, I_{sub} (OFF) for a single CMOS device will be,

$$I_{sub}(OFF)(A) = 100 \times \frac{7}{28} \times 10^{-9} \times 10^{\frac{-140}{60}} \quad (4.4)$$

$$I_{sub}(OFF)(A) = 1.25 \times 10^{-10} A$$

$$I_{sub}(OFF)(nA) = 0.125\ nA \quad (4.5)$$

The result obtained from equation (4.4) is then compared with those obtained for a typical 65 nm technology Silicon-based CMOS transistor, for the dimensions; L= 65 nm and W= 90 nm in order to illustrate its efficacy. In the comparison data, the Drain Induced Barrier Lowering coefficient, ɳ, was set at ɳ =0.1 and the subthreshold swing, S, at S =100 mV per decade (Lale, *et.al*., 2017, Weste, *et.al*., 2016). When the threshold voltage, V_{th}= 300 mV, the OFF-state subthreshold leakage current, I_{sub} (OFF) = 100 nA, whereas when the threshold voltage, V_{th}= 400 mV, the OFF-state subthreshold leakage current, I_{sub} (OFF) = 10 nA, and for the

threshold voltage, V_{th}= 500 mV, the OFF-state subthreshold leakage current, I_{sub} (OFF) = 1.0 nA.

In another comparison (Peng, 2016), the transistor parameters used were: Transistor effective length, L= 20.7 nm, Channel Width, W= 6.5 nm, the subthreshold swing, S, was set at S =83 mV per decade. When the threshold voltage, V_{th}= 170 mV, the OFF-state subthreshold leakage current, I_{sub} (OFF) = 3.8 nA.

The result obtained in equation (4.4) indicates a comparatively reduced OFF-state leakage current. This reduction in leakage current will result in the CMOS device's high performance speed and lower power consumption.

CHAPTER FIVE

CONCLUSION AND RECOMMENDATIONS

5.1 Conclusion

In this research, modelling and optimization of the OFF-state Subthreshold leakage current, I_{sub}(OFF), in a Silicon-based CMOS transistor was done based on the variations in the threshold voltage, V_{th} and the device dimensions, that is, the effective channel length, L and the effective channel width, W. A model equation (3.14), giving the relationship of these parameters, was derived and analysed using MATHCAD.

From the analysis of the model equation, it was observed that, for a Silicon-based CMOS transistor,

i) The OFF-state subthreshold leakage current, I_{sub} decreases exponentially with increase in the threshold voltage, V_{th}.

ii) The OFF-state subthreshold leakage current, I_{sub} , increases almost linearly with increase in the channel width, W, on first approximation.

iii) The OFF-state subthreshold leakage current, I_{sub} (OFF) decreases almost linearly, on first approximation, with increase in the effective transistor's channel length, L.

iv) To obtain a relatively low OFF-state subthreshold leakage current, I_{sub} (OFF) for a single CMOS transistor, the values of the parameters in the model equation (3.14) should be set at; the threshold voltage, V_{th} = 140 mV, the effective transistor channel length, L= 28 nm and the effective transistor width, W= 7nm.

5.2 Recommendations

The optimized values obtained in this research can be adopted by manufacturers of Silicon-based VLSI chips in order to take advantage of scaling of CMOS devices while still keeping the OFF-state subthreshold leakage current, I_{sub}(OFF) at a manageable minimum.

Future works also need to explore the possibility of varying the CMOS transistor's doping concentration so as to determine the relationship between the concentration and the OFF-state subthreshold leakage current, I_{sub}.

REFERENCES

Anis, M, Areibi, S. & Elmasry, M. (2003). "Design and Optimization of Multi-Threshold CMOS (MTCMOS) circuits". *IEEE transactions on Computer-Aided Design of Integrated Circuits and Systems,* Vol. 22 (10), New York, 1324- 1342.

Bohr, M. (2017). 14 nm Process Technology: Opening New Horizons. *Proceedings of the INTEL Technology and Manufacturing Day,* New York, 9-44.

Borkar, S. (1999). Design Challenges of Technology Scaling. *Proceedings of the IEEE Custom Integrated Circuits Conference,* New York, Vol. 10 (1), 23.

Butzen, P.F. & Ribas, R.P. (2007). Leakage current in sub micrometer CMOS gates. *Proceedings of the South symposium on microelectronics*, vol. 22, Porto Alegre, 47-50.

Cao, K. M. (2000). BSIM4 Gate Leakage Model including Source-Drain partition. *IEEE International Electron Devices Meeting (IEDM), Digest of technical papers*, New York, 815-818.

Chan, R. (2004). Advanced metal Gate/High-K dielectric stacks for high performance CMOS transistors. *Proceedings of AVS 5th International conference on Microelectronics and Interfaces,* New York, 3.

Deepaksubramanyan, B.S. & Nunez, A. (2007). Analysis of Subthreshold Leakage Reduction in CMOS Digital Circuits. *Proceedings of the 13th NASA VLSI Symposium*, Post Falls, Idaho, USA, 1-7.

Dutta, S. (2016). Recent advances in High Performance CMOS transistors: From Planar to Non Planar. *The Electrochemical Society Interface*, Pennsylvania State University, Vol. 10 (2), 41.

Gu, R.X. & Elmasry, M.I (1996). Power Dissipation analysis and optimization of Deep submicron CMOS digital circuits. *IEEE Journal of solid state circuits*, Vol. 31 (5), New York, 707-713.

Horiguchi, T.M. & Sakata, K.I. (1993). Switched-Source-Impedance CMOS Circuit for Low Standby Subthreshold Current Giga-Scale LSI's. *IEEE Journal of solid state circuits*, Vol. 28 (11), New York, 1131-1135.

Inukai, T. M. (2000). Boosted Gate MOS (BGMOS): Device/ Circuit Cooperation Scheme to Achieve Leakage-Free Giga-Scale Integration. *Proceedings of the IEEE Custom Integrated Circuits Conference*, New York, 409-412.

Kao, J., Narendra, S. & Chandrakasan, A. (2002). Subthreshold Leakage Modeling and Reduction Techniques. *IEEE Journal*, New York, 141-148.

Kawaguchi, H., Nose, K. & Sakurai, T. (2000). A Super-Cut Off CMOS (SCCMOS) Scheme for 0.5 V Supply Voltage with Pico-ampere Stand-by Current, *IEEE Journal of Solid State Circuits*, Vol. 35 (10), New York, 1498- 1501.

Kumar, M., Hussain, A. & Sajal, K. P. (2013). New Hybrid Digital Circuit Design Techniques for Reducing Subthreshold Leakage Power in Standby Mode. *Scientific Research Journal on Circuits and Systems,* Pradesh, India, 75- 82.

Lale, A., Grappin, A., Mazenq, L., Bourrier, D., Lecestre, A., Launay, J. & Temple-Boyer, P. (2017). Development of All-round SiO_2/ Al_2O_3 Gate, Suspended Silicon Nanowire Chemical Field Effect Transistors Si-nw-ChemFET. *Proceedings of the Eurosensors 2017 conference*, Vol. 1 (1), Paris, 419.

Maheshwari, S. (2014). Exploiting The Body Of MOS Devices For High Performance Analog Design. *International Journal of Advanced Research in Computer and Communication Engineering*, Vol. 3 (2), New York, 5695-5698.

Manisha, P. (2011). Analysis and Simulation of Subthreshold Leakage Current reduction in IP3 SRAM Bit-cell at 45nm CMOS technology for multimedia applications. *International Journal of Computer Theory and Engineering*, Vol. 3 (6), New York, 738.

Mookerjea, S. (2009). *IEEE International Electron Devices Meeting (IEDM), Digest of technical papers*, New York, 949.

Moore, G.E. (1965). Cramming more components onto integrated circuits. *Electronics*. New York: McGraw Hill Inc., 144.

Mukhopadhay, S. (2005). Accurate Estimation of Total Leakage in Nanometer-Scale Bulk CMOS circuits based on Device Geometry and Doping Profile. *IEEE Trans. On CAD of IC and Systems*, Vol. 24 (3), New York, 363-381.

Mutoh, S. (1995). 1-V Power Supply High-Speed Digital Circuit Technology with Multithreshold-Voltage CMOS. *IEEE Journal of solid state circuits*, New York, Vol. 30 (8).

Narendra, S. & Chandrakasan, A. (2006). Scaling of Stack Effect and its Application for Leakage Reduction. *International Symposium on Low Power Electronics and Design*, New York, Vol. 5 (3), 195-200.

Peng, Z. (2016). Advanced MOSFET Structures and Processes for Sub- 7nm CMOS Technologies. Doctor of Philosophy Thesis, University of California at Barkeley, 2016, 9-11.

Powell, M. (2001). Reducing Leakage in a High-Performance Deep-Submicron Instruction Cache. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 9 (1), New York, 134- 145.

Roy, K. & Prasad, S. C. (2007). Leakage current mechanisms and leakage reduction techniques in Deep sub-micrometer CMOS circuits. *Proceedings of IEEE*, Vol. 91 (2), New York, 305-327.

Sakata, T. (1994). Subthreshold-Current Reduction Circuits for Multi-Gigabit DRAMs. *IEEE Journal of solid state circuits*, Vol. 29, (7), 678- 693.

Saxena, N. & Soni, S. (2013). Leakage Current reduction in CMOS circuits using Stacking Effect. *International Journal of Application or Innovation in Engineering and Management (IJAIEM)*, Vol. 2 (11), 213.

Sharma, P. K., Bhargava, B. & Akashe, A. (2013). Reduction of leakage power in digital logic circuits using stacking technique in 45 nanometer Regime. *International Journal of Electrical, Computer, Energetic, Electronic and Communication Engineering*, Vol. 5 (3), 434- 453.

Sheu, B. J. (1987). BSIM: Berkeley Short-Channel IGFET Model for MOS transistors**.** *IEEE journal of Solid State Circuits,* Vol. SC-22, (No. 4), New York, 558-566.

Singh, S. K., Kaushik, B. K., Chauhan, D. S. & Kumar, S. (2013). Reduction of Subthreshold Leakage in MOS transistors. *World Applied Science Journal*, Vol. 3, Idosi Publications, 447.

Sreenivasulu, P. (2013). Power scaling in CMOS circuits by Dual-Threshold Voltage Technique. *International Journal of Engineering and Innovative Technology (IJEIT)*, Vol. 3 (1*)*, 128- 133.

Sundararajan, V. & Keshab, K. P. (1999). Low Power Synthesis of Dual Threshold Voltage CMOS VLSI Circuits. *International Symposium on Low Power Electronics and Design*, New York, Vol. 5 (3), 115.

Sze, S. M. & Ng, K. K. (2007). Physics of Semiconductor Devices. New Jersey: John Wiley and Sons Inc., 349.

Taur, Y. & Ming, T. H. (1998). Fundamentals of Modern VLSI Devices. New York: Cambridge University Press, 94- 95.

Tyagi, S. (2007). Moore's law: A CMOS scaling perspective. *Proceedings of the 14th International symposium on the Physical and Failure Analysis of the Integrated Circuits*, New York, Vol. 5 (6), 10-15.

Vijayalakshmi, D. (2017). Estimation of New Accurate Subthreshold and Gate Leakage Current. *International Journal of Exploring Emerging Trends in Engineering (IJEETE)*, New York, Vol. 1 (1), 8-21.

Weste, N. H. & Harris, D. M. (2016). CMOS VLSI Design: A Circuits and Systems Perspective. 4th Edition. Boston: Addison-Wesley Inc., 61-87.

Xu, Y. J., Luo, Z. Y., Li, X. W., Li, L. J. & Hong, X. L. (2004). Leakage Current Estimation of CMOS Circuits With Stack Effect. *12th IEEE Asian Test Symposium*, Xian, China, Vol. 19 (5), 708- 717.

Yadav, S. & Ramola, V. (2015). Reduction Of Leakage Power In CMOS Circuits (Gates) Using Variable Body Biasing With Sleep Insertion Technique. *International Journal of Engineering Development and Research*, Dehradun, Vol. 3 (3), 1-6.

Yang, E. (1988). Microelectronic Devices. New York: McGraw Hill Inc., 209-296.

APPENDIX

Drain Induced Barrier Lowering (DIBL)

Typically, the channel depletion region is solely due to the applied gate voltage, and that all depletion charge beneath the gate originates from the MOS field effects. This ignores the depletion regions of the source and the reverse-biased drain junction, which become important with shrinking channel lengths. In a short channel device, however, the source and drain depletion width in the vertical direction and the source-drain potential have a strong effect on the band bending over a significant portion of the device.

Therefore, the threshold voltage, and consequently the subthreshold current of short-channel devices vary with the drain bias. This effect is referred to as the Drain Induced Barrier Lowering (DIBL). Since a part of the region below the gate is already depleted by the source and drain fields, a smaller threshold voltage suffices to cause strong inversion. Thus, the zero-bias threshold voltage, V_{tho}, decreases with L for short-channel devices.

The DIBL effect is more pronounced in short-channel transistors. It can be modeled as (Weste, *et.al*., 2016),

$$V_{th} = V_{tho} - \eta V_{ds} \qquad \text{(A 1.0)}$$

where, η is the Drain Induced Barrier Lowering (DIBL) Coefficient and V_{ds} is the drain-to-source voltage.

A similar effect is obtained by raising the drain-to-source voltage, V_{ds}, as this increases the width of the drain-junction depletion region. Consequently, V_{th}

decreases with increasing V_{ds}; causing V_{th} to be a function of V_{ds}, as shown in Figure A1.

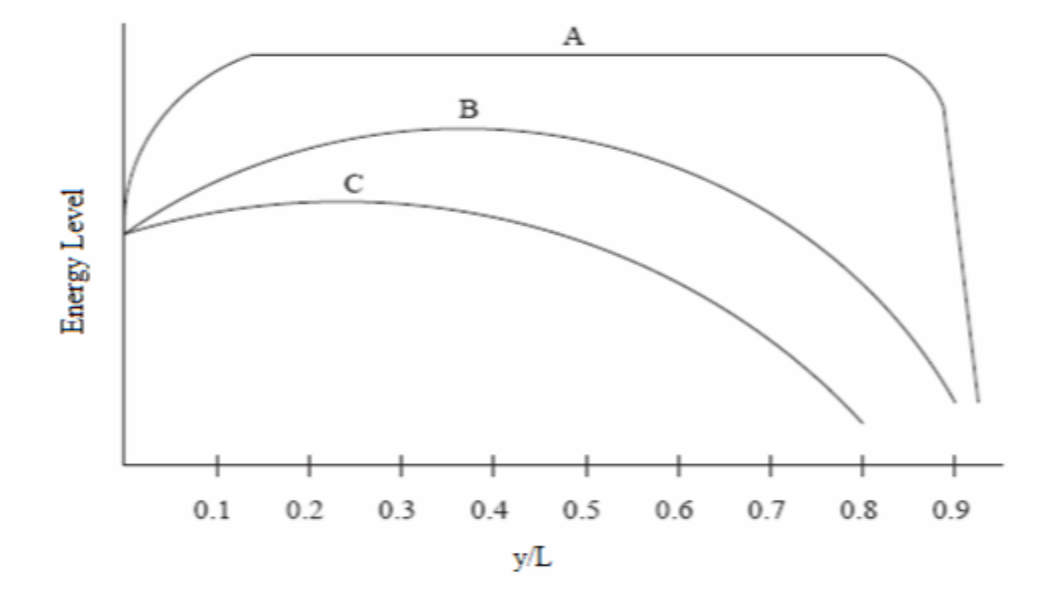


Figure A 1: Drain Induced Barrier Lowering (DIBL) for low L.

For high enough values of V_{dd}, the source and drain regions can even be shorted together, and normal device operation ceases to exist. DIBL, thus, occurs when the depletion regions of the drain and source interact with each other near the channel surface to lower the source potential.

DIBL is enhanced at high drain voltages and shorter channel lengths. The surface DIBL typically occurs before the deep bulk punchthrough. Ideally, DIBL does not change the subthreshold slope, S, but does lower V_{th}.

Tables of Results

Table A1: Variation of I_{sub} (L) and Channel length L

$L := 10..28$

Subthreshold slope S= 60 (Isub1 (L)), 90 (Isub2 (L)), 120 (Isub3 (L)).

$$Isub1(L) := 100 \cdot \frac{7}{L} \cdot 10^{-9} \cdot 10^{-5}$$

$$Isub2(L) := 100 \cdot \frac{7}{L} \cdot 10^{-9} \cdot 10^{-3.3}$$

$$Isub3(L) := 100 \cdot \frac{7}{L} \cdot 10^{-9} \cdot 10^{-2.5}$$

L =	Isub1 (L) =	Isub2 (L) =	Isub3 (L) =
10	$7 \cdot 10^{-13}$	$3.508 \cdot 10^{-11}$	$2.214 \cdot 10^{-10}$
11	$6.364 \cdot 10^{-13}$	$3.189 \cdot 10^{-11}$	$2.012 \cdot 10^{-10}$
12	$5.833 \cdot 10^{-13}$	$2.924 \cdot 10^{-11}$	$1.845 \cdot 10^{-10}$
13	$5.385 \cdot 10^{-13}$	$2.699 \cdot 10^{-11}$	$1.703 \cdot 10^{-10}$
14	$5 \cdot 10^{-13}$	$2.506 \cdot 10^{-11}$	$1.581 \cdot 10^{-10}$
15	$4.667 \cdot 10^{-13}$	$2.339 \cdot 10^{-11}$	$1.476 \cdot 10^{-10}$
16	$4.375 \cdot 10^{-13}$	$2.193 \cdot 10^{-11}$	$1.383 \cdot 10^{-10}$
17	$4.118 \cdot 10^{-13}$	$2.064 \cdot 10^{-11}$	$1.302 \cdot 10^{-10}$
18	$3.889 \cdot 10^{-13}$	$1.949 \cdot 10^{-11}$	$1.23 \cdot 10^{-10}$
19	$3.684 \cdot 10^{-13}$	$1.846 \cdot 10^{-11}$	$1.165 \cdot 10^{-10}$
20	$3.5 \cdot 10^{-13}$	$1.754 \cdot 10^{-11}$	$1.107 \cdot 10^{-10}$
21	$3.333 \cdot 10^{-13}$	$1.671 \cdot 10^{-11}$	$1.054 \cdot 10^{-10}$
22	$3.182 \cdot 10^{-13}$	$1.595 \cdot 10^{-11}$	$1.006 \cdot 10^{-10}$
23	$3.043 \cdot 10^{-13}$	$1.525 \cdot 10^{-11}$	$9.624 \cdot 10^{-11}$
24	$2.917 \cdot 10^{-13}$	$1.462 \cdot 10^{-11}$	$9.223 \cdot 10^{-11}$
25	$2.8 \cdot 10^{-13}$	$1.403 \cdot 10^{-11}$	$8.854 \cdot 10^{-11}$
26	$2.692 \cdot 10^{-13}$	$1.349 \cdot 10^{-11}$	$8.514 \cdot 10^{-11}$
27	$2.593 \cdot 10^{-13}$	$1.299 \cdot 10^{-11}$	$8.198 \cdot 10^{-11}$
28	$2.5 \cdot 10^{-13}$	$1.253 \cdot 10^{-11}$	$7.906 \cdot 10^{-11}$

Table A 2: Variation of I_{sub} (W) and Channel width W

$W := 7..32$

Subthreshold slope S= 60 (Isub1 (W)), 90 (Isub2 (W)), 120 (Isub3 (W)).

$$Isub1(W) := 100 \cdot \frac{W}{10} \cdot 10^{-9} \cdot 10^{-5}$$

$$Isub2(W) := 100 \cdot \frac{W}{10} \cdot 10^{-9} \cdot 10^{-3.3}$$

$$Isub3(W) := 100 \cdot \frac{W}{10} \cdot 10^{-9} \cdot 10^{-2.5}$$

W =	Isub1 (W) =	Isub2 (W) =	Isub3 (W) =
7	$7 \cdot 10^{-13}$	$3.508 \cdot 10^{-11}$	$2.214 \cdot 10^{-10}$
8	$8 \cdot 10^{-13}$	$4.009 \cdot 10^{-11}$	$2.53 \cdot 10^{-10}$
9	$9 \cdot 10^{-13}$	$4.511 \cdot 10^{-11}$	$2.846 \cdot 10^{-10}$
10	$1 \cdot 10^{-12}$	$5.012 \cdot 10^{-11}$	$3.162 \cdot 10^{-10}$
11	$1.1 \cdot 10^{-12}$	$5.513 \cdot 10^{-11}$	$3.479 \cdot 10^{-10}$
12	$1.2 \cdot 10^{-12}$	$6.014 \cdot 10^{-11}$	$3.795 \cdot 10^{-10}$
13	$1.3 \cdot 10^{-12}$	$6.515 \cdot 10^{-11}$	$4.111 \cdot 10^{-10}$
14	$1.4 \cdot 10^{-12}$	$7.017 \cdot 10^{-11}$	$4.427 \cdot 10^{-10}$
15	$1.5 \cdot 10^{-12}$	$7.518 \cdot 10^{-11}$	$4.743 \cdot 10^{-10}$
16	$1.6 \cdot 10^{-12}$	$8.019 \cdot 10^{-11}$	$5.06 \cdot 10^{-10}$
17	$1.7 \cdot 10^{-12}$	$8.52 \cdot 10^{-11}$	$5.376 \cdot 10^{-10}$
18	$1.8 \cdot 10^{-12}$	$9.021 \cdot 10^{-11}$	$5.692 \cdot 10^{-10}$
19	$1.9 \cdot 10^{-12}$	$9.523 \cdot 10^{-11}$	$6.008 \cdot 10^{-10}$
20	$2 \cdot 10^{-12}$	$1.002 \cdot 10^{-10}$	$6.325 \cdot 10^{-10}$
21	$2.1 \cdot 10^{-12}$	$1.052 \cdot 10^{-10}$	$6.641 \cdot 10^{-10}$
22	$2.2 \cdot 10^{-12}$	$1.103 \cdot 10^{-10}$	$6.957 \cdot 10^{-10}$
23	$2.3 \cdot 10^{-12}$	$1.153 \cdot 10^{-10}$	$7.273 \cdot 10^{-10}$
24	$2.4 \cdot 10^{-12}$	$1.203 \cdot 10^{-10}$	$7.589 \cdot 10^{-10}$
25	$2.5 \cdot 10^{-12}$	$1.253 \cdot 10^{-10}$	$7.906 \cdot 10^{-10}$
26	$2.6 \cdot 10^{-12}$	$1.303 \cdot 10^{-10}$	$8.222 \cdot 10^{-10}$
27	$2.7 \cdot 10^{-12}$	$1.353 \cdot 10^{-10}$	$8.538 \cdot 10^{-10}$
28	$2.8 \cdot 10^{-12}$	$1.403 \cdot 10^{-10}$	$8.854 \cdot 10^{-10}$
29	$2.9 \cdot 10^{-12}$	$1.453 \cdot 10^{-10}$	$9.171 \cdot 10^{-10}$
30	$3 \cdot 10^{-12}$	$1.504 \cdot 10^{-10}$	$9.487 \cdot 10^{-10}$
31	$3.1 \cdot 10^{-12}$	$1.554 \cdot 10^{-10}$	$9.803 \cdot 10^{-10}$
32	$3.2 \cdot 10^{-12}$	$1.604 \cdot 10^{-10}$	$1.012 \cdot 10^{-9}$

Table A 3: Variation of I_{sub} (V_{th}) and Threshold voltage V_{th}

$Vth := 0..300$ $\quad Isub1(Vth) := 100 \cdot 7.0 \cdot 10^{-8} \cdot 10^{\frac{-Vth}{60}}$ Subthreshold slope S= 60 (Isub1 (Vth)), 90 (Isub2 (Vth)), 120 (Isub3 (Vth)).

$Isub2(Vth) := 100 \cdot 7.0 \cdot 10^{-8} \cdot 10^{\frac{-Vth}{90}}$

$Isub3(Vth) := 100 \cdot 7.0 \cdot 10^{-8} \cdot 10^{\frac{-Vth}{120}}$

Vth =	Isub1 (Vth) =	Isub2 (Vth) =	Isub3 (Vth) =
0	$7 \cdot 10^{-6}$	$2.271 \cdot 10^{-7}$	$7 \cdot 10^{-6}$
1	$6.736 \cdot 10^{-6}$	$2.214 \cdot 10^{-7}$	$6.867 \cdot 10^{-6}$
2	$6.483 \cdot 10^{-6}$	$2.158 \cdot 10^{-7}$	$6.736 \cdot 10^{-6}$
3	$6.239 \cdot 10^{-6}$	$2.103 \cdot 10^{-7}$	$6.608 \cdot 10^{-6}$
4	$6.004 \cdot 10^{-6}$	$2.05 \cdot 10^{-7}$	$6.483 \cdot 10^{-6}$
5	$5.778 \cdot 10^{-6}$	$1.998 \cdot 10^{-7}$	$6.36 \cdot 10^{-6}$
6	$5.56 \cdot 10^{-6}$	$1.948 \cdot 10^{-7}$	$6.239 \cdot 10^{-6}$
7	$5.351 \cdot 10^{-6}$	$1.899 \cdot 10^{-7}$	$6.12 \cdot 10^{-6}$
8	$5.149 \cdot 10^{-6}$	$1.851 \cdot 10^{-7}$	$6.004 \cdot 10^{-6}$
9	$4.956 \cdot 10^{-6}$	$1.804 \cdot 10^{-7}$	$5.89 \cdot 10^{-6}$
10	$4.769 \cdot 10^{-6}$	$1.758 \cdot 10^{-7}$	$5.778 \cdot 10^{-6}$
11	$4.589 \cdot 10^{-6}$	$1.714 \cdot 10^{-7}$	$5.668 \cdot 10^{-6}$
12	$4.417 \cdot 10^{-6}$	$1.671 \cdot 10^{-7}$	$5.56 \cdot 10^{-6}$
13	$4.25 \cdot 10^{-6}$	$1.628 \cdot 10^{-7}$	$5.455 \cdot 10^{-6}$
14	$4.09 \cdot 10^{-6}$	$1.587 \cdot 10^{-7}$	$5.351 \cdot 10^{-6}$
15	$3.936 \cdot 10^{-6}$	$1.547 \cdot 10^{-7}$	$5.249 \cdot 10^{-6}$
16	$3.788 \cdot 10^{-6}$	$1.508 \cdot 10^{-7}$	$5.149 \cdot 10^{-6}$
17	$3.646 \cdot 10^{-6}$	$1.47 \cdot 10^{-7}$	$5.052 \cdot 10^{-6}$
18	$3.508 \cdot 10^{-6}$	$1.433 \cdot 10^{-7}$	$4.956 \cdot 10^{-6}$
19	$3.376 \cdot 10^{-6}$	$1.397 \cdot 10^{-7}$	$4.861 \cdot 10^{-6}$
20	$3.249 \cdot 10^{-6}$	$1.361 \cdot 10^{-7}$	$4.769 \cdot 10^{-6}$
21	$3.127 \cdot 10^{-6}$	$1.327 \cdot 10^{-7}$	$4.678 \cdot 10^{-6}$
22	$3.009 \cdot 10^{-6}$	$1.293 \cdot 10^{-7}$	$4.589 \cdot 10^{-6}$
23	$2.896 \cdot 10^{-6}$	$1.261 \cdot 10^{-7}$	$4.502 \cdot 10^{-6}$
24	$2.787 \cdot 10^{-6}$	$1.229 \cdot 10^{-7}$	$4.417 \cdot 10^{-6}$
25	$2.682 \cdot 10^{-6}$	$1.198 \cdot 10^{-7}$	$4.333 \cdot 10^{-6}$
26	$2.581 \cdot 10^{-6}$	$1.168 \cdot 10^{-7}$	$4.25 \cdot 10^{-6}$
27	$2.484 \cdot 10^{-6}$	$1.138 \cdot 10^{-7}$	$4.17 \cdot 10^{-6}$
28	$2.39 \cdot 10^{-6}$	$1.109 \cdot 10^{-7}$	$4.09 \cdot 10^{-6}$
29	$2.3 \cdot 10^{-6}$	$1.081 \cdot 10^{-7}$	$4.013 \cdot 10^{-6}$
30	$2.214 \cdot 10^{-6}$	$1.054 \cdot 10^{-7}$	$3.936 \cdot 10^{-6}$